

IMPLEMENTATION OF A MODERN CONTROL ALGORITHM
ON A GENERAL PURPOSE MICROCOMPUTER

by

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ABSTRACT

IMPLEMENTATION OF A MODERN CONTROL ALGORITHM ON A GENERAL PURPOSE MICROCOMPUTER

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This thesis presents an implementation of a modern control algorithm on a microcomputer. The digital controller uses both classical and modern control techniques to improve the tracking accuracy of a closed-loop system. Integral control is used to achieve a zero steady-state error to a constant reference input. To improve the transient response of the system, state-variable feedback compensation is used with a one-step predictor to estimate the state vector from a single measurement and to account for computational delay. This technique is then applied to a second order system. Results are presented which indicate that the controller works properly. However, an unsatisfactory response can be easily tuned up by adjusting a few parameters in the software program used.

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LIST OF SYMBOLS

SYMBOL	DEFINITION
$G(s)$	Open-loop analog transfer function
$G(z)$	Zero-Order-Hold equivalent of $G(s)$
A	Continuous system matrix
B	Continuous control input matrix
C	Continuous or discrete output matrix
D	Continuous plant direct transmission matrix
Φ	Discrete plant system matrix
Γ	Discrete plant control input matrix
X	Plant state vector
U	Control signal
R	Reference input
T_m	Sampling period
D_o	Numerator of integral controller
$A_c(z)$	Desired closed-loop characteristic polynomial
$\alpha_0, \dots, \alpha_{f^m+1}$	Coefficients of $A_c(z)$
$\hat{X}$	Estimate of actual state, X
$\hat{G}(z)$	$Y(z)/V(z)$
M	Controller reference-input distribution matrix
N	Controller reference-input direct transmission matrix

K	Control gain matrix
L	Estimator gain matrix
Σ	Analog or binary adder
V	Output of integral controller
$X(k)$	Kth sample of X
R_k	Kth sample of R
T_s	Active cycle of sampling clock
"n"	System type, equal to poles at the origin
τ	"Dummy" variable of integration
$a_0, \dots, a_{p-1}$	Numerator coefficients of $G(s)$
$b_0, \dots, b_{p-1}$	Denominator coefficients of $G(s)$
$c_0, \dots, c_{p-1}$	Numerator coefficients of $G(z)$ and $G(z)$
$d_0, \dots, d_{p-1}$	Denominator coefficients of $G(z)$
$h_0, \dots, h_{p-1}$	Denominator coefficients of $G(z)$
$\tilde{X}$	$X - \hat{X}$

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CHAPTER I

INTRODUCTION

1.1 Background

A widely used method for shaping the dynamic response of a closed loop system is state variable feedback. According to this method, the eigenvalues of the closed loop system can be placed anywhere one wishes in the complex s plane provided that the original system is controllable and that all the state variables are accessible for direct measurement.

In a number of design problems, the state vector is not accessible to measurement. However, it is possible in many such problems to implement control by using output rather than state feedback if an additional dynamical system known as a state observer or estimator is introduced. In this case, the original system has to be both controllable and observable. Furthermore, the separation principle states that the dynamics of the state variable feedback controller are independent of the dynamics of the estimator and vice versa [2]. Consequently, the controller and the observer may be designed separately.

1.2 Objective and approach

The purpose of this thesis is to present an

application of the separation principle to the tracking problem. Using an integral digital compensator along with a one-step predictor [1] (i.e., a state observer in which the estimate is one cycle ahead of the measurement) to be used with a state variable control law, a second order type "0" system gets converted to a third order type "1" system. The digital compensator as well as the observer and state-variable feedback algorithms are programmed in BASIC on a TRS-80 Model IV microcomputer, which is interfaced to the given plant. The design is carried out using Program CC, a PC-based interactive computer-aided control system design program.

1.3 Overview

Chapter II of this thesis is devoted to interfacing. It shows how a TRS-80 Model IV microcomputer is connected to an analog system in order to control it efficiently using a modern control algorithm.

Chapter III is the heart of this thesis. The tracking problem is introduced, and the design steps to develop the state model and implement the proposed control algorithm are clearly presented.

In Chapter IV, the technique developed in Chapter III is applied to a second order system. The simulation results from CC and data collected from the plots obtained with a Primeline X-Y plotter and the photographs of the oscilloscope display are presented and discussed. Also, the

sensitivity of the system to variations of the compensator and observer gain matrices was studied, and conclusions were drawn.

Finally, in Chapter V, a brief summary of the thesis is given and some suggestions for further work on the design are presented.

The interested reader should also turn his attention to the Appendices, which contain the data sheets of the special chips used in the project along with a proof.

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CHAPTER II

MICROCOMPUTER INTERFACING

2.1 Introduction

This chapter deals mainly with the hardware built and the software used to interface a TRS-80 Model IV microcomputer to an analog plant, which is simulated using an operational amplifier circuit. The interface specifications are given and the various components of the interfacing circuit are discussed.

2.2 Interface Specifications

Since a one-step predictor is to be employed to estimate the state vector to be used in the control law, the interface requirements are:

- A). The interface should provide for a single-input single-output operation.
- B). The operating ranges for the analog input and output should be 0-5 volts.
- C). The output of the analog plant should be sampled at the same time its input gets updated.
- D). The sampling frequency should be held constant, and it should be determined by the frequency of a real-time clock interfaced to the system.
- E). The interface should provide for a reference input.

2.3 Hardware and Software Description

A block diagram of the interface system that can be used to satisfy all the specifications described in section 2.2 is shown in Figure 2.1 below.

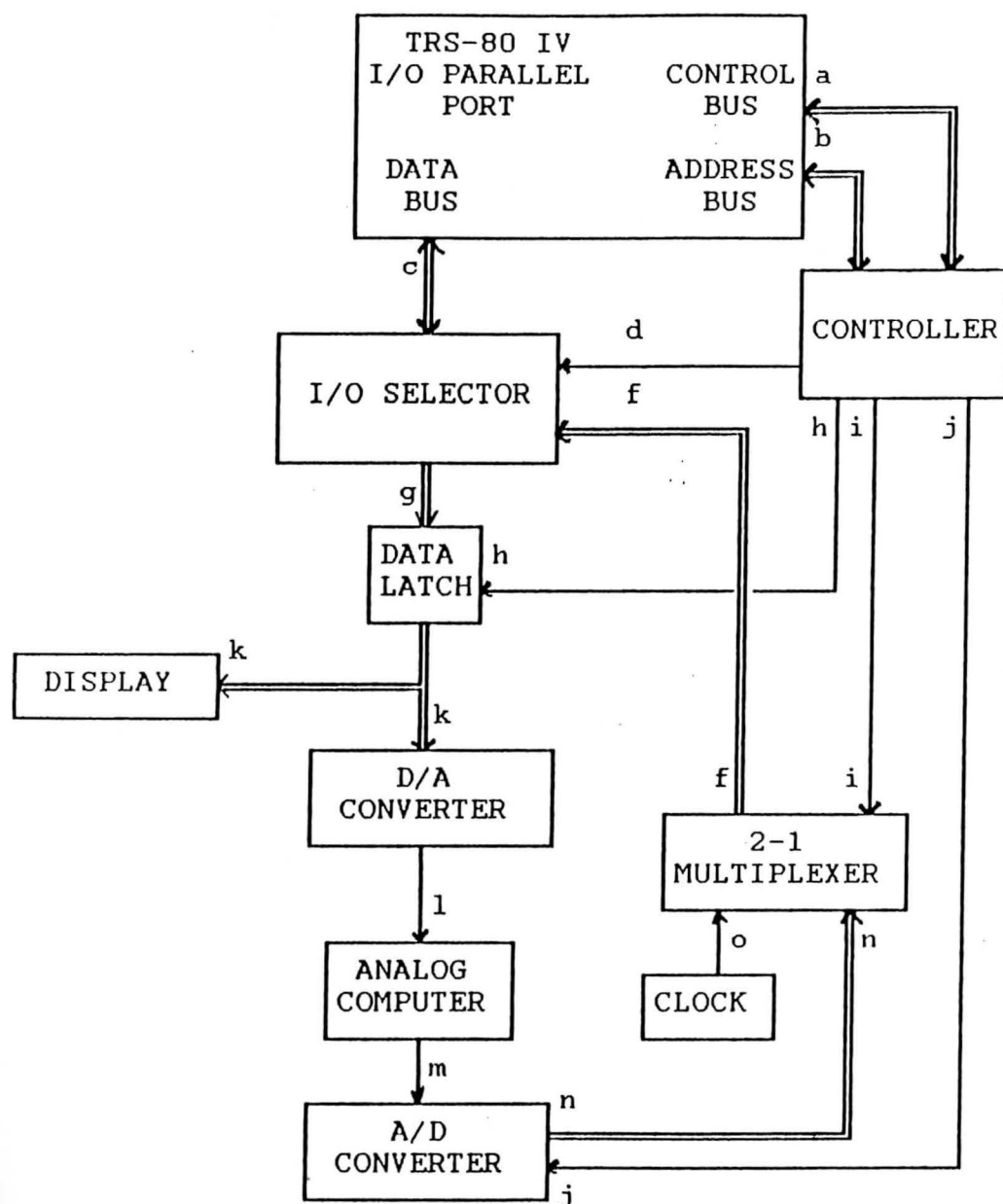


Fig. 2.1 Interface Block Diagram.

Following is a brief description of each of the components of the interface system as well as their circuit diagram.

A) TRS-80 Model IV computer [3] is an 64K 8-bit microcomputer with two built-in disk drives, a monitor, and a keyboard. Among others, it features a parallel I/O bus which supports all the signals necessary to interface to a device compatible with the Z80's I/O structure. That is:

- ♦ Address Bus ($A_0 - A_7$).
- ♦ Data Bus ($D_0 - D_7$).
- ♦ Control Lines (an asterisk denotes an asserted low signal):
 - $IN^*(L)$: an input is in progress;
 - $OUT^*(L)$: an output is in progress;
 - $RESET^*(L)$: system reset;
 - $IOBUSINT^*(L)$: I/O Bus is interrupted;
 - $IOBUSWAIT^*(L)$: forces wait stages on the Z80;
 - $EXIOSEL^*(L)$: input to CPU allowing data to be read;
 - $M1^*(L)$: Z80 signal;
 - $IORQ^*(L)$: Z80 signal.

B) I/O Selector is designed to configure the computer's I/O port either as an input or as an output port. This is accomplished using two bi-directional bus drivers 8216 [6] as shown in Figure 2.2. A "0" at $DIEN^*$ pin will allow data to flow from DI's to the computer's Data Bus. Otherwise, data is being sent from the Data Bus to the Data

Latches.

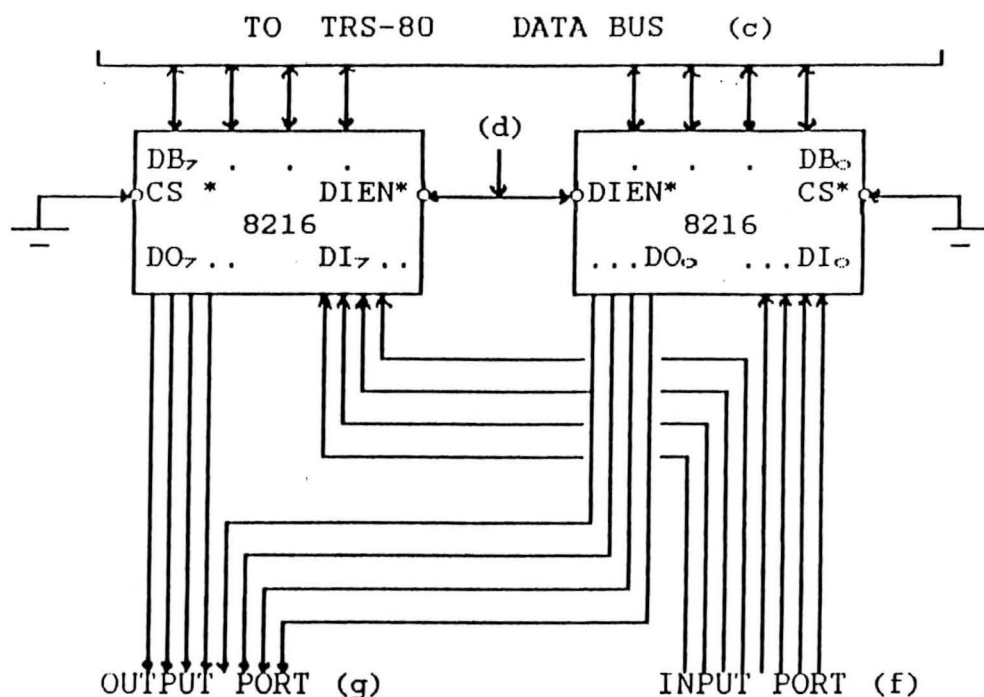


Fig. 2.2 I/O Selector Circuit Diagram.

C) The Data Latch is a 74100 8-bit D-Latch flip flop [8]. It is used for temporary data storage. Data gets updated every T_m seconds. The circuit diagram of this component is shown in Figure 2.3.

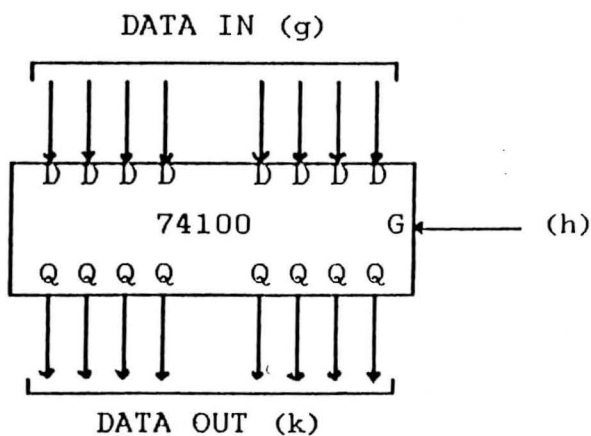


Fig. 2.3 An 8-Bit Data Latch Flip Flop.

D) The next component is the 8-bit LED Display. Its purpose is to display the contents of the Data Bus during an output operation.

E) The DAC0806 current output Digital to Analog Converter [see Appendix B] is one of the most important elements of the interface circuit. It is the heart of any sampling system as it converts a sequence of digital numbers to a staircase analog signal. In a control system, it acts as a Zero Order Hold.

To provide for a 0 to 5V operation, a current-to-voltage converter has been added to it as shown in the circuit diagram [7] of Figure 2.4.

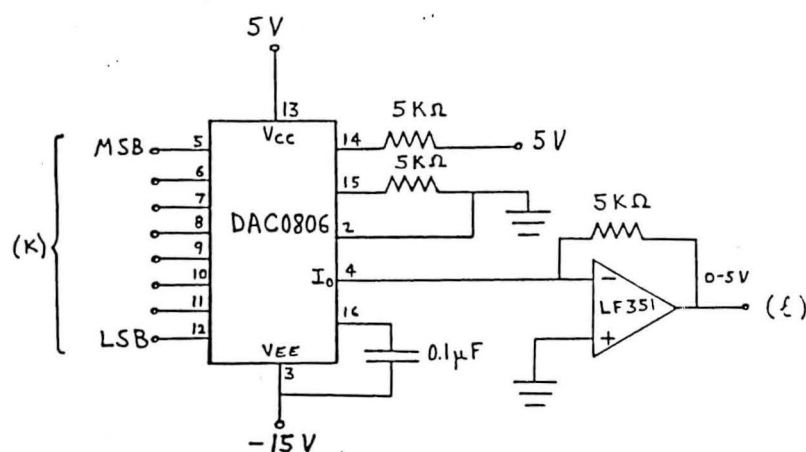


Fig. 2.4 A 0-5V Digital to Analog Converter.

F) An analog computer can be easily built using operational amplifier circuits, which simulate the desired transfer functions. For example, a function of the form

$$G(s) = \frac{A}{s^2 + Bs + C} \quad \{2.1\}$$

may be realized using the three amplifier biquad [5] shown in Figure 2.5, where

$$A = \frac{1}{R_2 R_4 C_1 C_2} \quad B = \frac{1}{R_1 C_1} \quad C = \frac{1}{R_2 R_3 C_1 C_2}$$

Also, $R_5 = R_6$ and $V_{out} = V_2$.

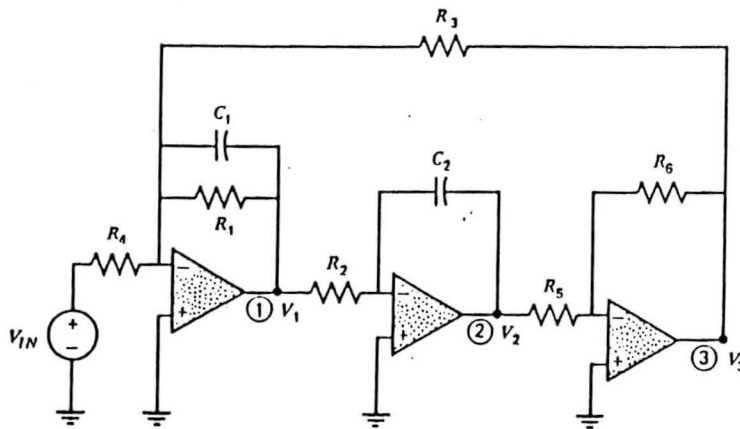


Fig. 2.5 Circuit Realization of {2.1}.

G) A Digital Control System would not be complete without an Analog to Digital Converter. Here, the 8-bit ADC0804LCN [see Appendix A] is being employed. For a 0 to 5V analog input, the circuit [4] shown in Figure 2.6 may be used.

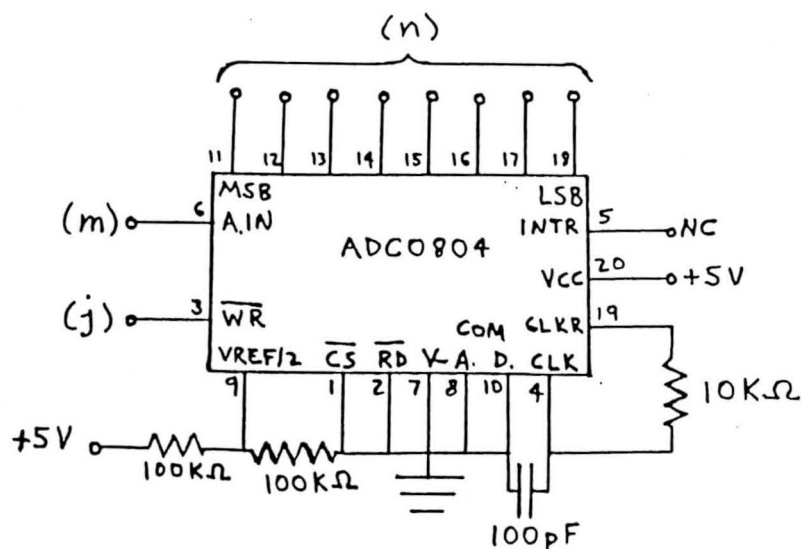


Fig. 2.6 A 0-5V Analog to Digital Converter.

H) The 74157 [8] 2-to-1 Multiplexer shown in Figure 2.7 is used to achieve a real-time clock operation. This device is configured so that data may be transferred to the data bus of the computer only at the rising edge of the clock, which is one of the two inputs.

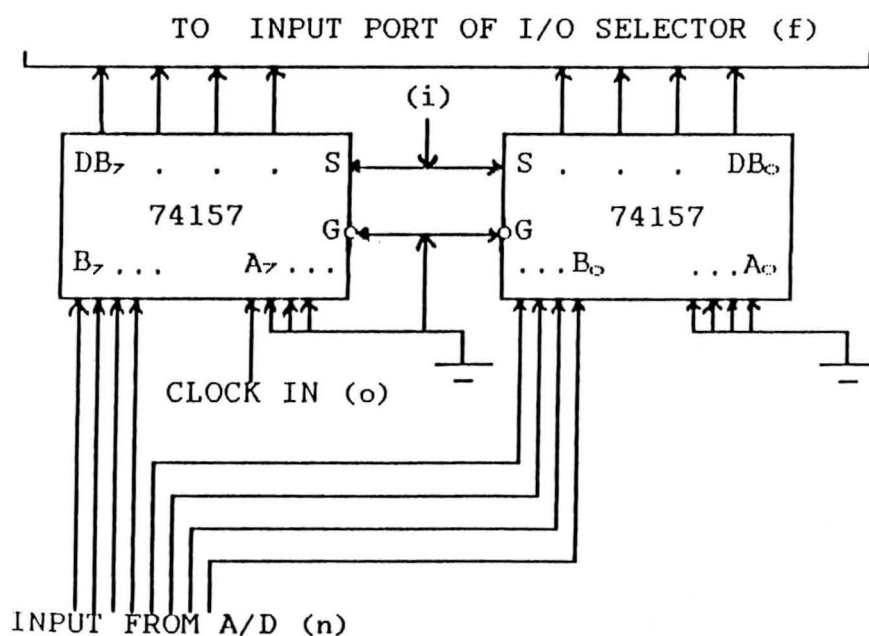


Fig. 2.7 A 2-to-1 Multiplexer.

I) The clock is an important element of the interface because its period, T_m , determines the sampling frequency of the control system. Also, its active cycle (see Figure 2.8) must be carefully set. That is, T_m must be long enough to be read by the computer, and short enough to ensure a real-time clock operation.

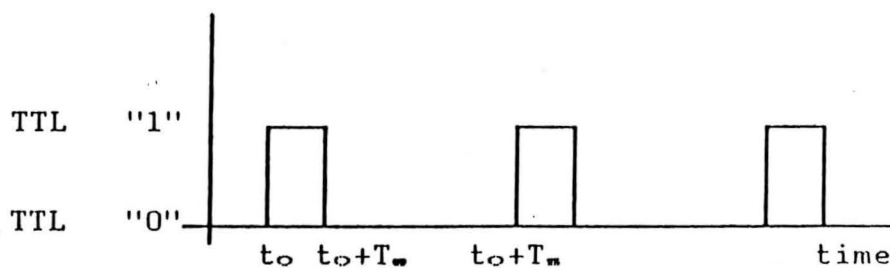


Fig. 2.8 Clock Characteristics.

J) Finally, the most important part of the hardware circuit is the controller (see Figure 2.9). It is used to regulate the flow of data from/to the analog system to/from the data bus of the microcomputer in such a way so that no information is lost.

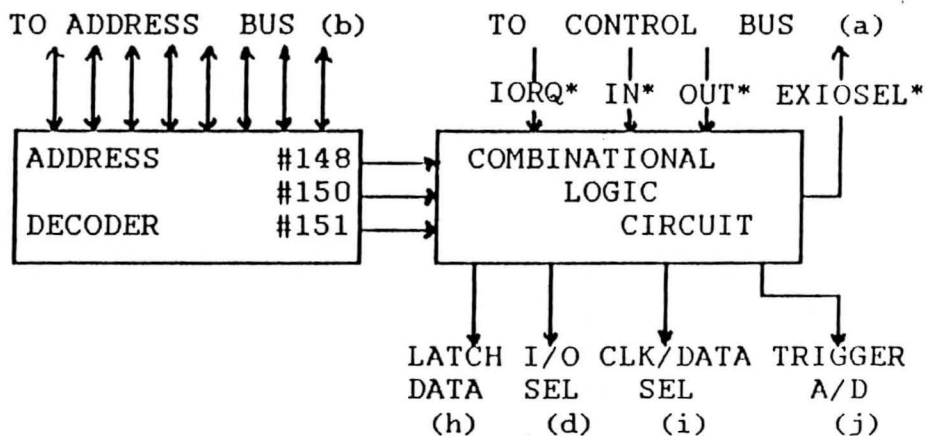


Fig. 2.9 Controller Block Diagram

The equations governing the combinational logic circuit are

$$\text{LATCH DATA} = \text{OUT} \cdot \text{IORQ} \cdot (\#148)$$

$$\text{EXIOSEL} = (\#150 + \#151) \cdot \text{IN} \cdot \text{IORQ}$$

$$\text{I/O SEL} = \text{EXIOSEL} \cdot$$

$$\text{CLK/DATA SEL} = (\#150) \cdot \text{IN} \cdot \text{IORQ}$$

$$\text{TRIGGER A/D} = (\text{LATCH DATA}) \cdot$$

where, "." stands for an "AND" operation and "+" stands for an "OR" operation.

The controller performs the following functions:

- ♦ with a BASIC statement,

```
300 OUT 148,Uk
```

the control Uk gets updated, and the A/D converter starts the conversion;

- ♦ with the following statements,

```
100 IF INP(150)><128 THEN GOTO 100
```

```
110 Yin = INP(151)
```

```
120 REM The rising edge of the clock is detected
```

```
130 REM Continue calculations
```

```
      .      .
```

```
      .      .
```

```
500 REM Start new cycle
```

```
510 GOTO 100
```

the rising edge of the clock [note that the most significant bit of the multiplexer input is connected to the clock] is detected (in address 150), and then the output of the analog system (in address 151) is sampled.

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CHAPTER III

THE TRACKING PROBLEM

3.1 Introduction

A system designed to follow a reference input is known as a tracking system [2]. Such systems are widely used in radars, autopilots, telescopes, ship navigation, and inertial guidance systems. In this chapter, a technique to design a tracking system to track a constant reference input is presented. This method uses an integral compensator to provide tracking accuracy and also state-variable feedback compensation to achieve the desired transient response. A one-step predictor is used to provide estimates of all the state variables from the single measurement and to allow for computational delay.

The type of a system is determined by the number of its poles at $s = 0$ in the s domain, or at $z = 1$ in the z domain. The significance of system type is that type " n " can track a polynomial input of degree $(n - 1)$ with zero steady-state error. Thus, type " 1 " performance is required to track a constant reference input accurately.

3.2 The Design Approach.

Using integral control, a type " 0 " plant can be made to exhibit a type " 1 " behavior. A discretized closed loop

system incorporating an outer loop with integral compensation and an inner loop using state-variable feedback is shown in Figure 3.1. In this system, the reference input R_k can be provided for by a statement in the BASIC program used. The design approach used here is based on pole placement; i.e., the controller parameters are selected to give desired closed-loop poles, which are roots of a selected characteristic polynomial $A_c(z)$.

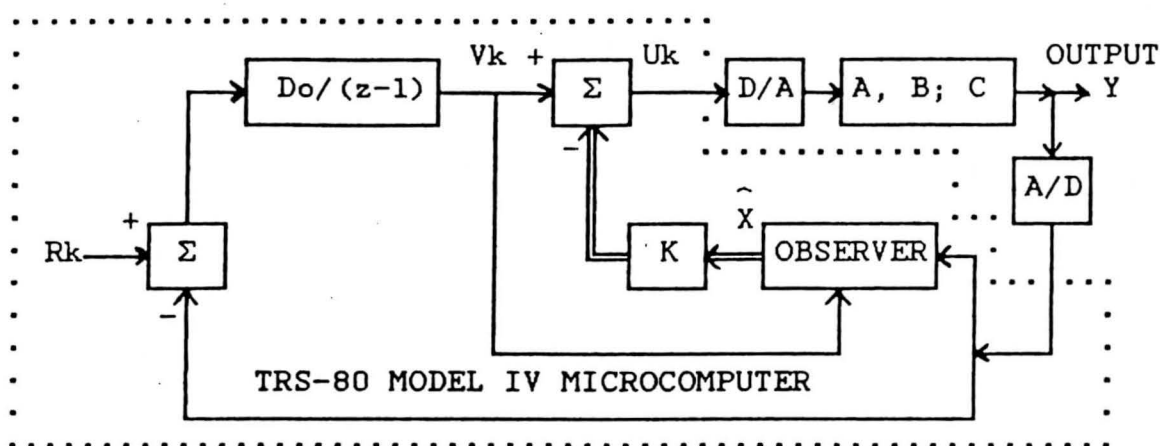


Fig. 3.1 Closed Loop System.

To determine the values of the controller parameters, the following steps are taken:

Step 1. Starting with the transfer function of the analog system,

$$G(s) = \frac{a_{p-1} s^{p-1} + \dots + a_1 s + a_0}{s^p + b_{p-1} s^{p-1} + \dots + b_1 s + b_0} \quad \{3.1\}$$

its Zero-Order-Hold Equivalent, $G(z)$, is calculated at the desired sampling frequency:

$$G(z) = \frac{c_{p-1} z^{p-1} + \dots + z c_1 + c_0}{z^p + d_{p-1} z^{p-1} + \dots + d_1 z + d_0} \quad \{3.2\}$$

This $G(z)$ is equivalent to $G(s)$ in the sense that the values of the discrete output of $G(z)$ are exact samples of the analog output of $G(s)$ when a digital-to-analog converter (which acts as a Zero-Order-Hold) is used to provide the analog input to $G(s)$.

Step 2. Next, the state space model of $G(s)$ is realized using the following observable canonical form [11]:

$$\frac{dX}{dt} = \underbrace{\begin{bmatrix} -b_{p-1} & 1 & 0 & \dots & 0 \\ -b_{p-2} & 0 & 1 & \dots & 0 \\ -b_{p-3} & 0 & 0 & \dots & 0 \\ \vdots & & & & \vdots \\ -b_0 & 0 & 0 & \dots & 0 \end{bmatrix}}_A X + \underbrace{\begin{bmatrix} a_{p-1} \\ a_{p-2} \\ a_{p-3} \\ \vdots \\ a_0 \end{bmatrix}}_B U \quad \{3.3\}$$

$$Y = \underbrace{\begin{bmatrix} 1 & 0 & 0 & \dots \end{bmatrix}}_C X \quad \{3.4\}$$

Step 3. The state space system shown above is then checked for controllability and observability. It is imperative that this system is both observable and controllable if a state variable feedback compensator with a one-step predictor is to be used. In this case, there is no problem unless $G(s)$ is not reduced.

Step 4. The next step is to get the discretized model of the analog state space model

$$X(k+1) = \Phi(T_m) X(k) + \Gamma(T_m) U(k) \quad \{3.5\}$$

$$Y(k) = C X(k) \quad \{3.6\}$$

using the same sampling frequency, T_m , as in Step 1 above.

This is done using the following equations:

$$\Phi(T_m) = \exp(A T_m) \quad \{3.7\}$$

$$\Gamma(T_m) = \int_0^{T_m} \Phi(\tau) d\tau B \quad \{3.8\}$$

Step 5. Let

$$\hat{G}(z) \equiv \frac{Y(z)}{V(z)} \quad \{3.9\}$$

be the transfer function from the integrator output $V(k)$ to the plant output (see Figure 3.2). If state-variable feedback is used in the inner loop, $\hat{G}(z)$ will have the following form

$$\hat{G}(z) \equiv \frac{c_{p-1} z^{p-1} + \dots + z c_1 + c_0}{z^p + h_{p-1} z^{p-1} + \dots + h_1 z + h_0} \quad \{3.10\}$$

Set the numerator of $\left[1 + \frac{D_0 \hat{G}(z)}{z - 1} \right]$ equal to the

desired closed-loop characteristic polynomial $A_c(z)$ and

solve for $h_0, h_1, \dots, h_{p-1}$, and D_0 . The order of $A_c(z)$ should be one more than that of the original system:

$$A_c(z) = z^{p+1} + \alpha_p z^p + \dots + \alpha_1 z + \alpha_0 \quad \{3.11\}$$

Step 6. At this point the integral controller is fully specified, and the state variable feedback compensator can be designed assuming that all the states are available for feedback (see Figure 3.2). The compensator gain matrix, K , can now be calculated using a) the Bass-Gura formula [2], b) Ackermann's formula [12], or c) the pole placement command of CC [10].

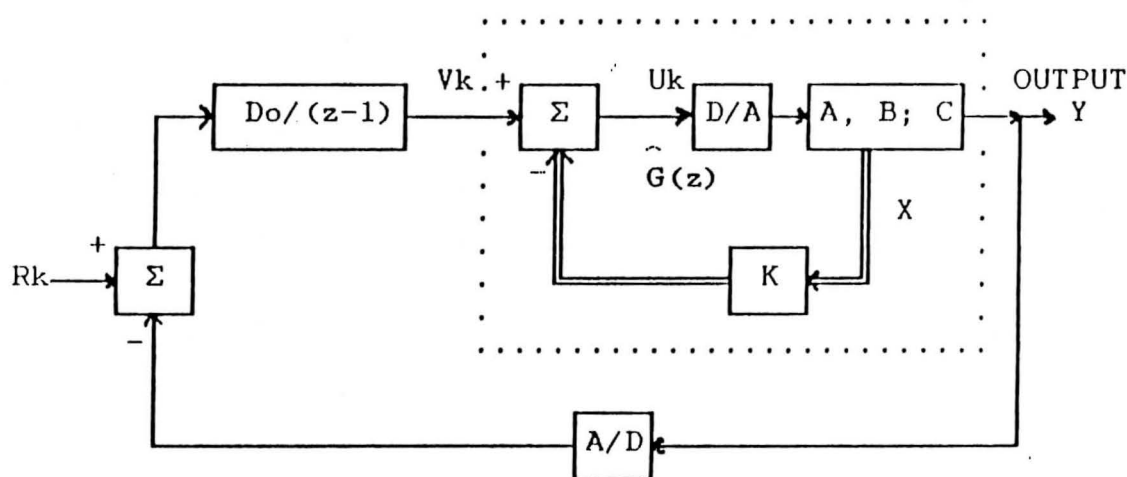


Fig. 3,2 State Variable Feedback

The poles are to be selected so that the inner-loop system $\hat{G}(z)$ has poles as computed in step 5.

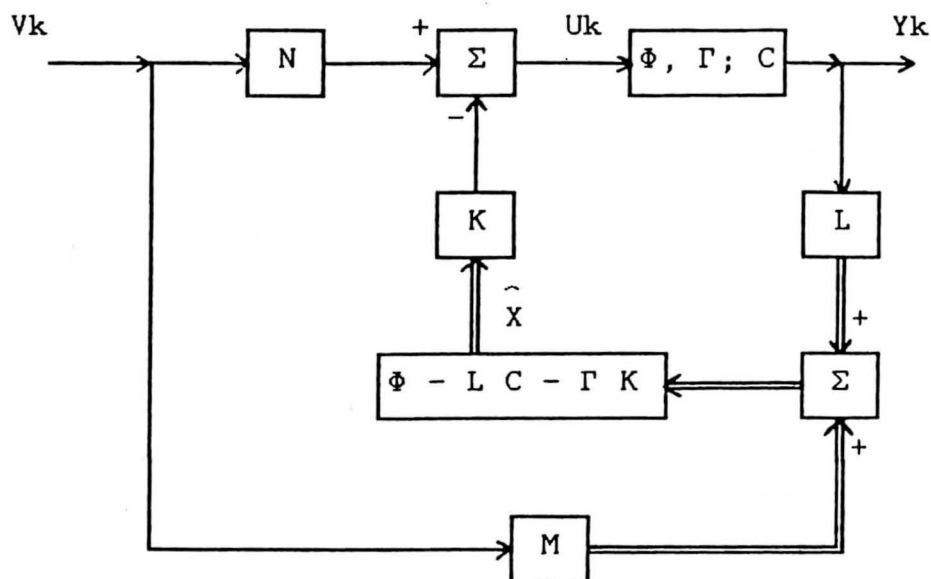


Fig. 3.3 Full-State Observer Details.

Step 7 The requirement that all the states of the open loop system be accessible for feedback can now be relaxed with the addition of the state-observer [1] of Figure 3.3. The observer is carefully designed so that its presence does not change $\hat{G}(z)$. This is accomplished [for proof, see Appendix C] by setting

$$N = 1 \quad \text{and} \quad M = N \Gamma = \Gamma \quad \{3.12\}$$

so that the added observer poles are cancelled by the feedforward zeroes [which were affected by M and N] of the overall transfer function from V to Y. Next, the observer poles are chosen so that the observer error dynamics are faster than the dynamics of the controlled plant. Using any of the techniques discussed in step 6, the observer gain matrix, L, can be found.

Step 8. The final state space model for the controller is the following:

$$U(k) = N V(k) - K \hat{X}(k) \quad \{3.13\}$$

$$V(k+1) = V(k) + D_0 (Rk - Y(k)) \quad \{3.14\}$$

$$\hat{X}(k+1) = (\Phi - L C - \Gamma K) \hat{X}(k) + L Y(k) + M V(k) \quad \{3.15\}$$

At this point, the design has been completed and the equations shown above can be programmed in the TRS-80 Model IV microcomputer to implement the control algorithm.

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CHAPTER IV

APPLICATION

4.1 Introduction

In this chapter, the design technique described in Chapter III is applied to a second order system. The system selected to be controlled has the following transfer function

$$G(s) = \frac{1}{s^2 + s + 1} \quad \{4.1\}$$

4.2 Model and Results

The function of {4.1} has poles at

$$s_1 = -0.5 + j 0.866 \quad \text{and} \quad s_2 = -0.5 - j 0.866 \quad \{4.2\}$$

The sampling period chosen is

$$T_s = 0.2 \text{ seconds.}$$

Also, the desired closed loop characteristic polynomial is:

$$A_c(s) = (s+1) (s^2 + 1.6 s + 1) \quad \{4.3\}$$

Discretizing at $T_s = 0.2$ seconds one obtains

$$A_c(z) = z^3 - 2.510762 z^2 + 2.111467 z - 0.5945206 \quad \{4.4\}$$

The discrete state space model of equation {4.1} calculated using the CC macro program of Table 4-2 is

$$X(k+1) = \Phi X(k) + \Gamma U(k)$$

$$Y(k) = C X(k)$$

where

$$\Phi = \begin{bmatrix} 0.8012668 & 0.1800640 \\ -0.1800640 & 0.9813308 \end{bmatrix} \quad \{4.5\}$$

$$\Gamma = \begin{bmatrix} 0.01866924 \\ 0.1987332 \end{bmatrix} \quad \{4.6\}$$

and

$$C = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad \{4.7\}$$

Also, the numerator coefficients of $G(z)$ are

$$c_0 = 0.017464 \quad \text{and} \quad c_1 = 0.01866924 \quad \{4.8\}$$

Using the BASIC program shown in Table 4-1, the following parameters can be determined:

$$h_1 = -1.510762 \quad \{4.9\}$$

$$h_0 = 0.5975097 \quad \{4.10\}$$

$$D_0 = 0.1711537 \quad \{4.11\}$$

Next, the parameters calculated above are put in the same CC macro program mentioned above, and the following compensator gain matrix, K , is computed:

$$K = \begin{bmatrix} 0.0363457 & 1.36443 \end{bmatrix} \quad \{4.12\}$$

The observer poles are then selected at:

$$z_1 = 0.7 + j 0.1 \quad \text{and} \quad z_2 = 0.7 - j 0.1$$

The corresponding observer gain matrix is then the following:

$$L = \begin{bmatrix} 0.385975 \\ 0.315121 \end{bmatrix} \quad \{4.13\}$$

Also,

$$\Phi - L C = \begin{bmatrix} 0.4186692 & 0.1800640 \\ -0.4950850 & 0.9813308 \end{bmatrix} \quad \{4.14\}$$

TABLE 4-1

BASIC PROGRAM USED TO CALCULATE h_0 , h_1 , D_0

```

10 CLS
15 REM   INPUT DATA FOLLOWS THIS LINE
20 C0 = 0.017464
30 C1 = 0.0186924
40 GA0 = -0.5945206
50 GA1 = 2.111467
60 GA2 = -2.510762
65 REM   NEXT, PERFORM CALCULATIONS
70 H1 = GA2 + 1
80 D0 = (GA1 + GA0 + H1) / (C0 + C1)
90 H0 = -GA0 + (C0 * D0)
100 REM   PRINT RESULTS
110 PRINT "H0 ="; H0
120 PRINT "H1 ="; H1
130 PRINT "D0 ="; D0
140 STOP
150 END

```

TABLE 4-2

CC MACRO PROGRAM LISTING

```

ANALOG
BUILD
2POLES,G,&5,&6
QUIT
CONVERT,G,G1,8,&1
ANALOG
STATE
OCF,G,P
PEXPONENTIAL,P,P1,&1,10
POLEPLACEMENT
P1
P2
3
1
1,&2,&3
2
&7,&8
&9,&10
UNPACK,P2,P3,P4,P5,P6
UNPACK,P1,P8,P9,P10,P11
MULTIPLY,P4,P10,P12
SUBTRACT,P8,P12,P13
PLPD,P13,"THIS IS ( $\Phi$  - L C) MATRIX: P13"
PLPD,P5,"THIS IS THE COMPENSATOR GAIN MATRIX: P5"
PLPD,P4,"THIS IS THE ESTIMATOR GAIN MATRIX: P4"
PLPD,P9,"THIS IS THE GAMMA MATRIX: P9"
IDENTITY,P7,1,-1
MULTIPLY,P7,P5,P14
IDENTITY,P15,1,1
AUGMENT,P4,P9,P16,1,0
AUGMENT,P6,P15,P17,1,0
PACK,P3,P16,P14,P17,P18
FADEEVA,P18,H1
EXTRACT,H1,G2,1,1
EXTRACT,H1,G3,1,2
QUIT
BUILD
G4=G1/(1-G2*G1)
G5=G3*G4
G6=&4/(Z-1)
G7=G6*G5
G8=G7/(1+G7)
G9=1-G8
G10=G9*G6
G11=(G10*G3)+(G8*G2)
QUIT

```

Finally, the program of Table 4-3 can be used to implement the control law on a Radio Shack TRS-80 Model IV microcomputer. The controller equations are contained in lines 190-230. Lines 190 and 200 are used to update the observer states; line 210 is used to update the discrete integrator; and line 230 contains the control calculation. Note that in the update of the observer state, the actual control U is used. This is to account for the saturation limits of the control (see lines 250 and 260).

TABLE 4-3

TRS-80 MODEL IV BASIC LISTING

```
5 CLS
7 REM      SYSTEM DESCRIPTION:
10 A11 = 0.418669
20 A12 = 0.180064
30 A21 = -0.495085
40 A22 = 0.981331
50 GAM1 = 0.01866924
60 GAM2 = 0.1987332
65 REM      COMPENSATOR GAINS:
70 K1 = 0.0363457
80 K2 = 1.36443
85 REM      OBSERVER GAINS:
90 L1 = 0.382598
100 L2 = 0.315021
105 REM
110 DO = 0.1711537
115 REM
120 INPUT; "ENTER REFERENCE INPUT (VOLTS)";RK
130 XH1=0: XH2=0:Y=0: UI=0: VK=0
140 OUT 148,0
150 IF INP(150)=0 THEN GOTO 150
160 OUT 148,UI
170 Y1 = INP(151)
180 Y = 0.0195313*Y1
190 NXH1 = A11*XH1 + A12*XH2 + L1*Y + GAM1*U
200 NXH2 = A21*XH1 + A22*XH2 + L2*Y + GAM2*U
210 VK1 = VK + DO*(RK-Y)
220 VK=VK1: XH1=NXH1: XH2=NXH2
230 U = VK - K1*XH1 - K2*XH2
240 YE = Y - XH1
250 IF U<0 THEN U=0
260 IF U>5 THEN U=5
270 UI = INT(U*51)
280 GOTO 150
290 STOP
300 END
```

Using Program CC's graphing capabilities, the system's open-loop and closed-loop responses were plotted. The results are shown in Figures 4.1, and 4.2.

In Figure 4.1, the output response of the closed-loop system is plotted. Both the transient and the steady-state responses look satisfactory. This suggests that the estimator works properly, estimating the states accurately without really making its presence noticeable. In other words, the separation principle holds. Also, Figure 4.2 shows the control signal applied to the input of the plant. As one would expect, the control signal settles to a nonzero but constant value in a finite amount of time. This is because the original system was of type "0" and it was converted to a type "1" to increase tracking accuracy to a constant step input. Another interesting observation is that the control signal does not saturate. This suggests that the controller implemented on the TRS-80 Model IV microcomputer should also work nicely. This is actually the case as it becomes obvious in the next series of plots shown in Figures 4.3 through 4.10, which were obtained using a Primeline X-Y plotter.

Figures 4.3 through 4.6 contain the plots corresponding to a 5V reference input while Figures 4.7 to 4.10 correspond to a 2.5V reference input.

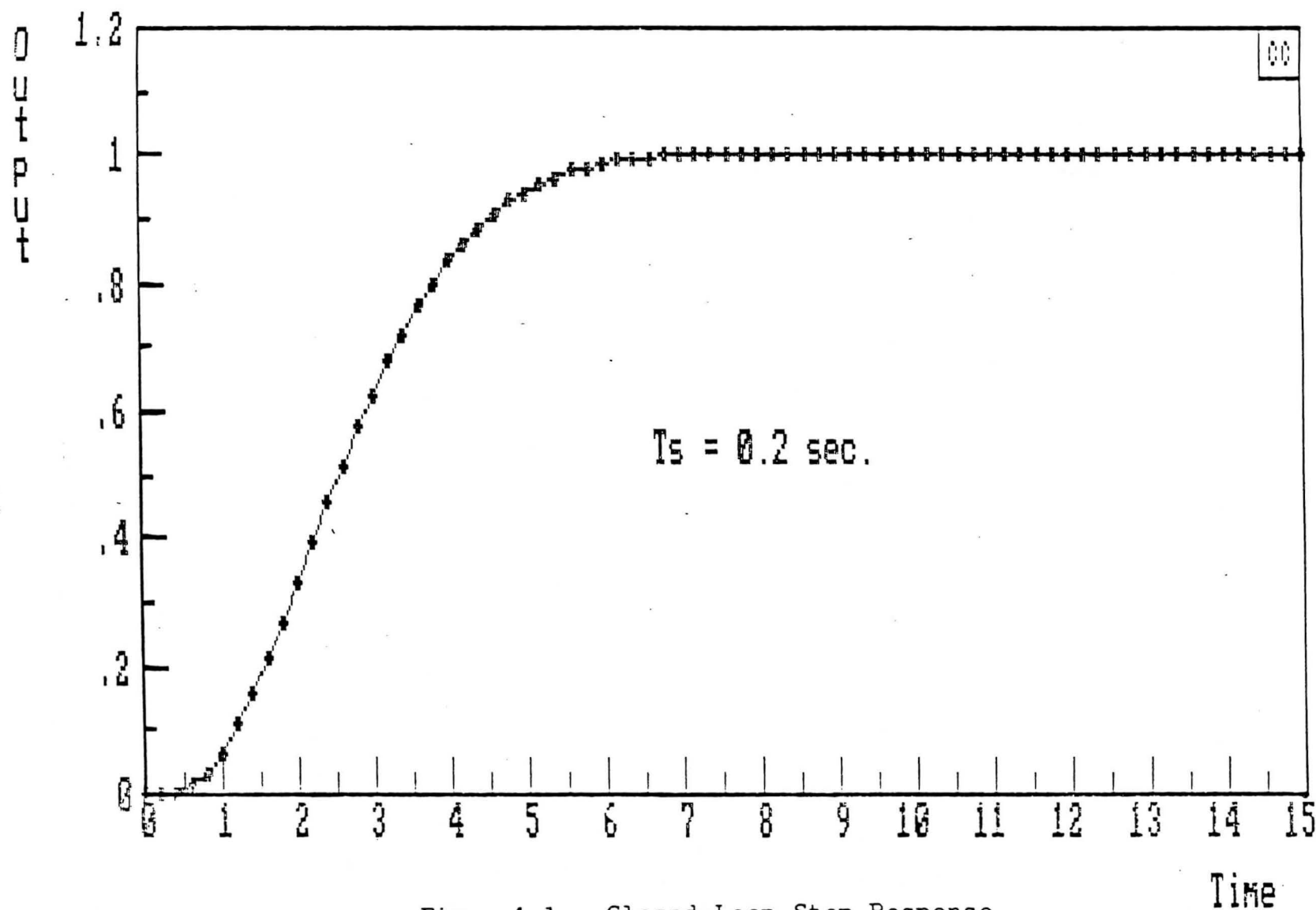


Fig. 4.1 Closed-Loop Step Response

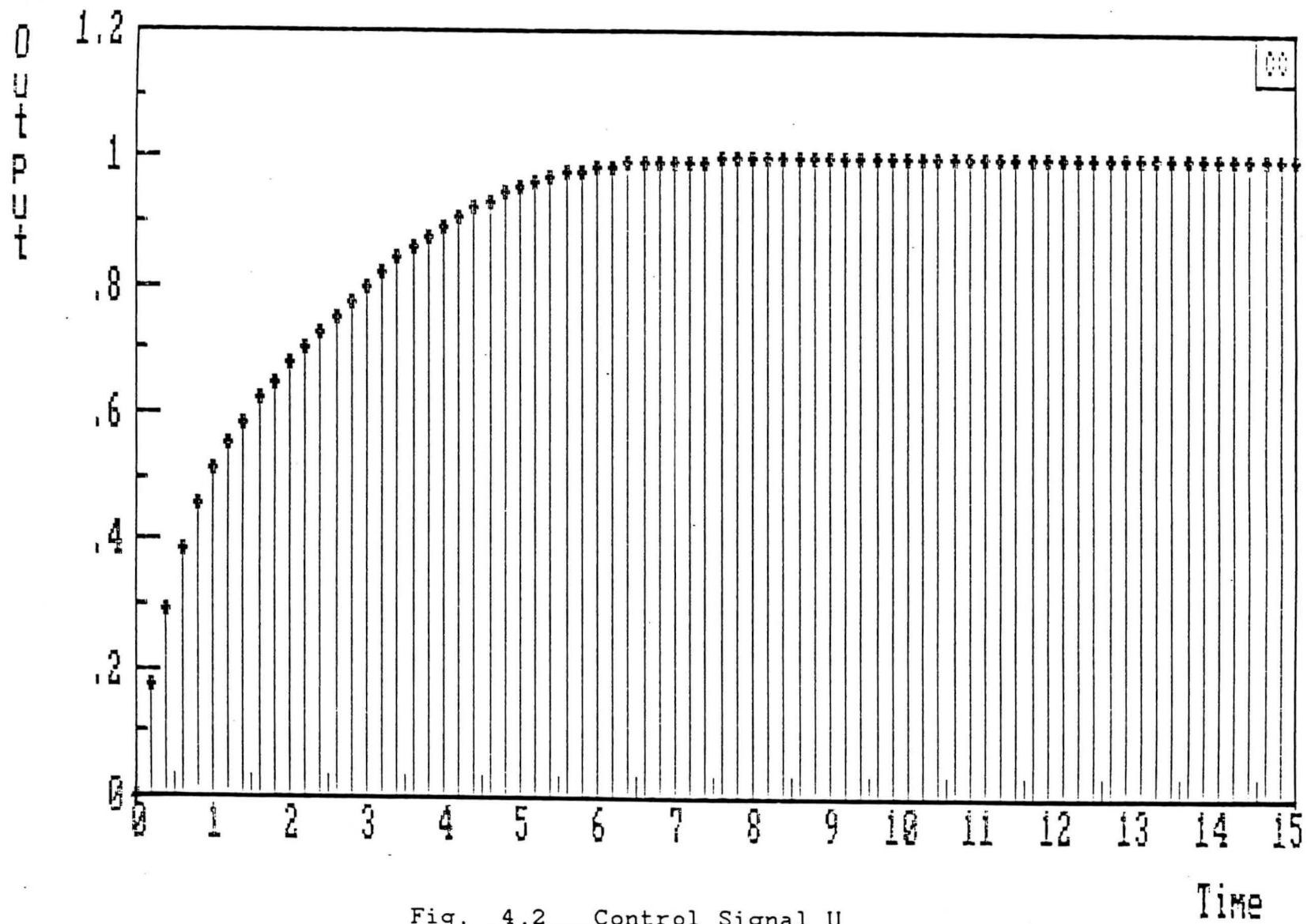


Fig. 4.2 Control Signal U

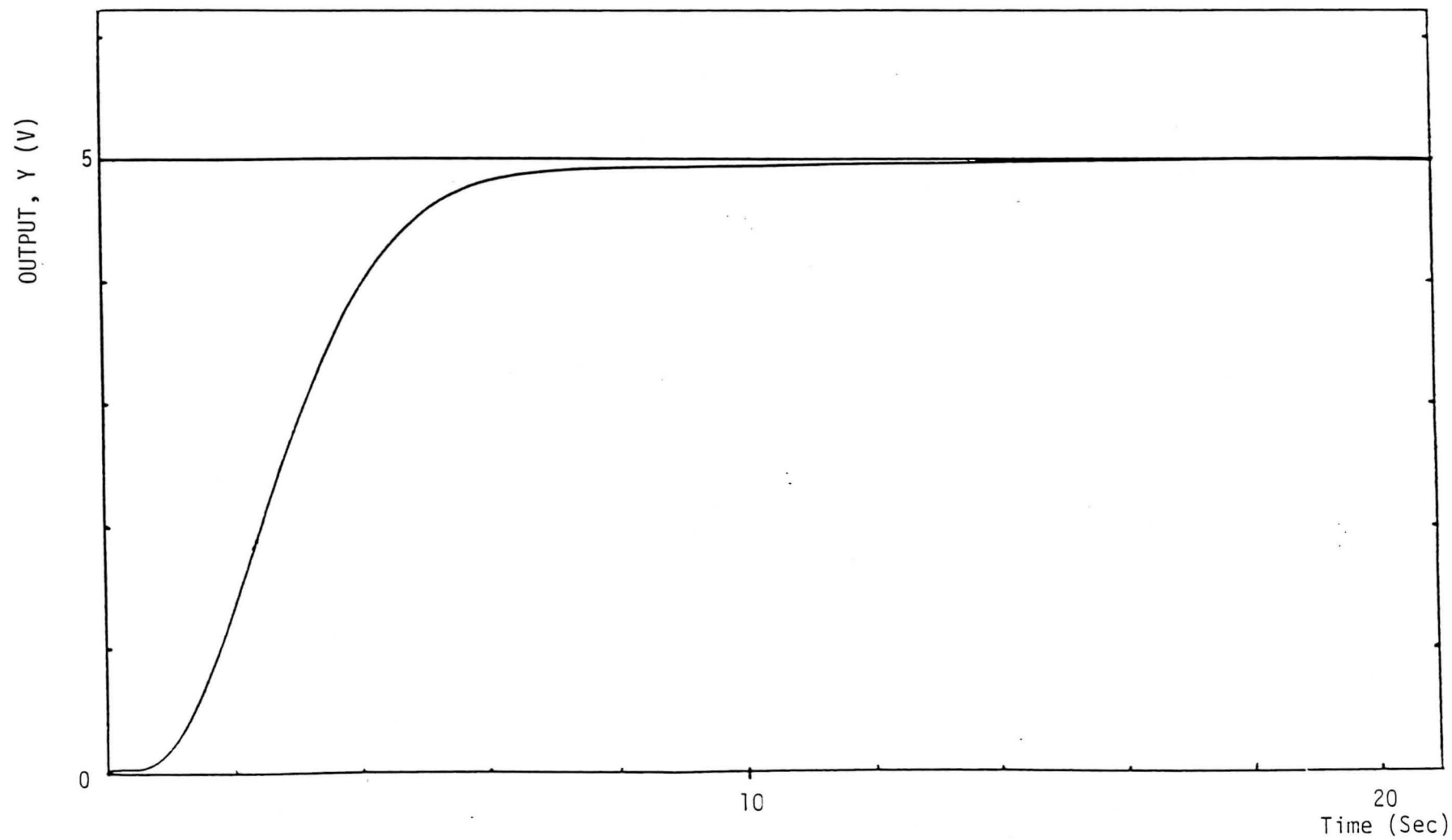


Fig. 4.3 Closed-Loop Step Response ($R_k=5V$)

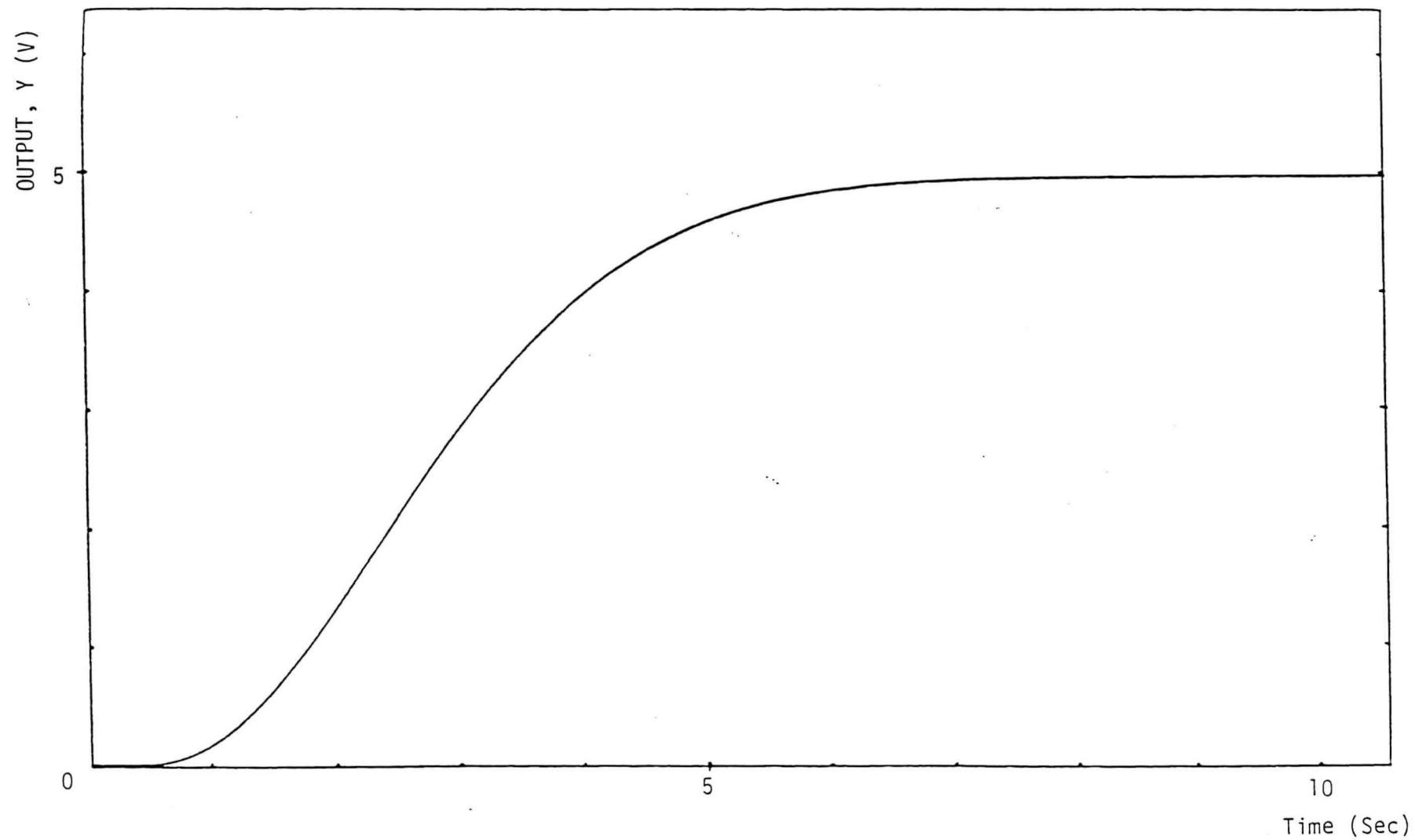


Fig. 4.4 Output Transient Response ($R_k=5V$)

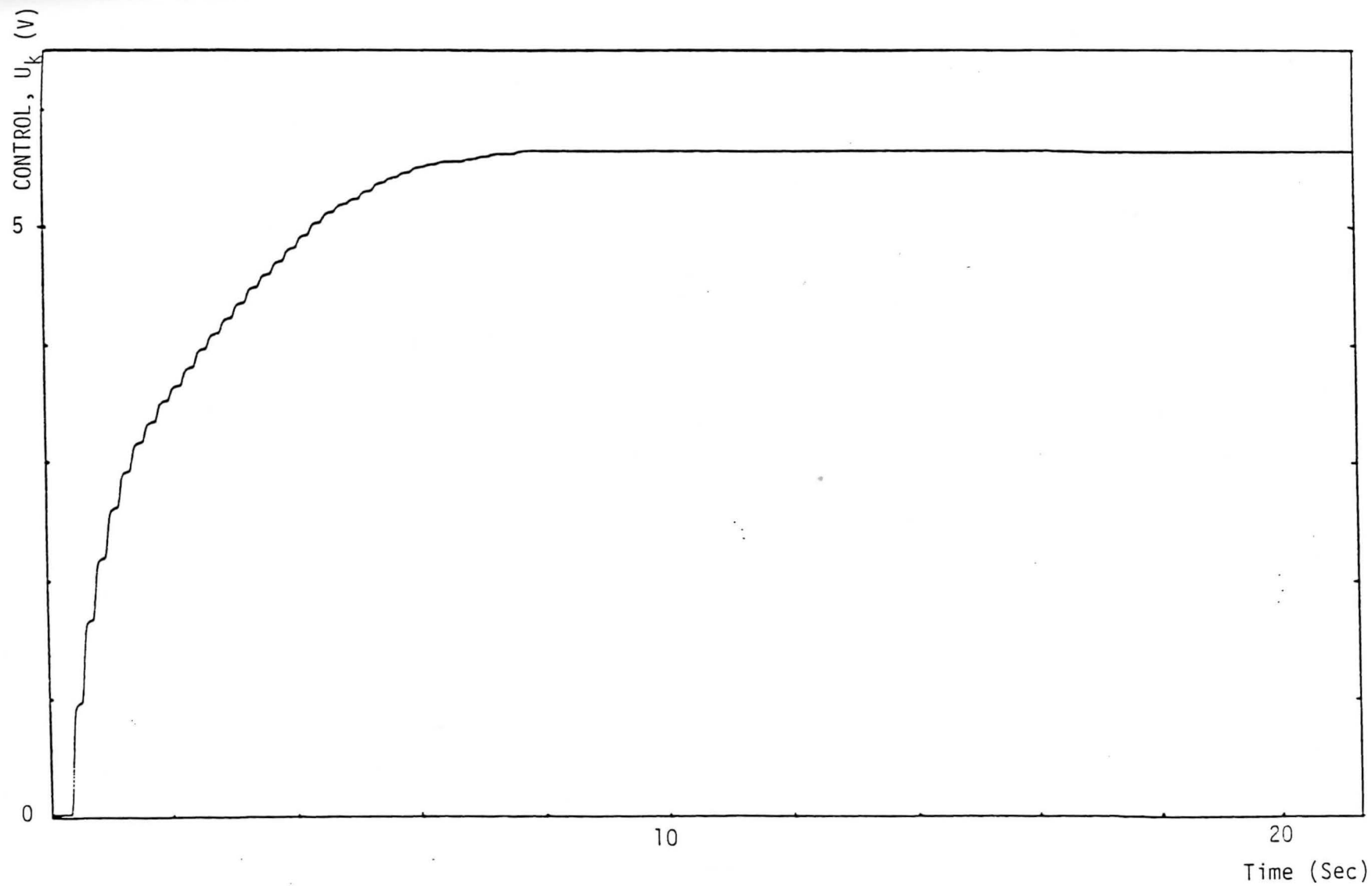


Fig. 4.5 Control Signal ($R_k=5V$)

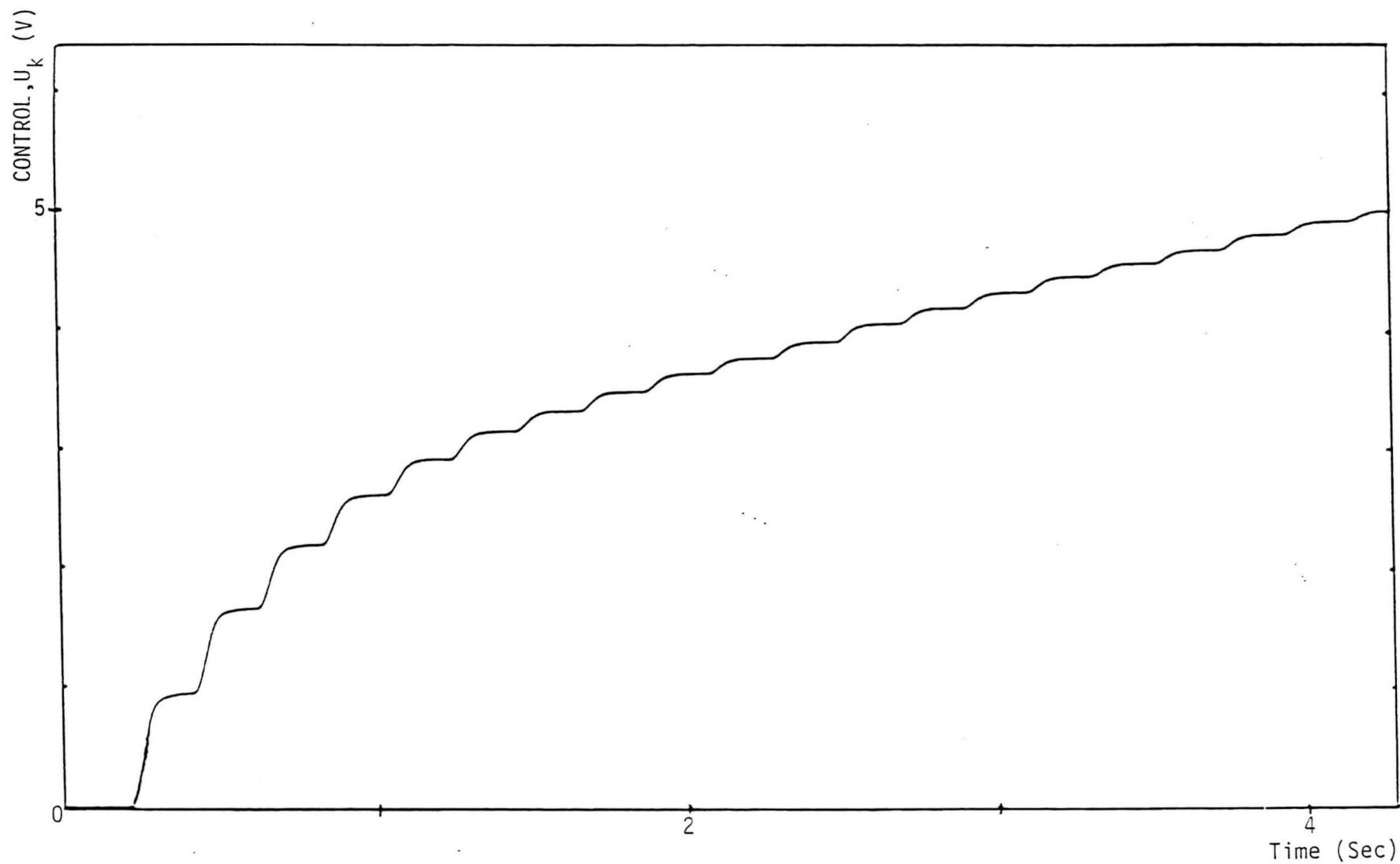


Fig. 4.6 Control Transient Response ($R_k=5V$)

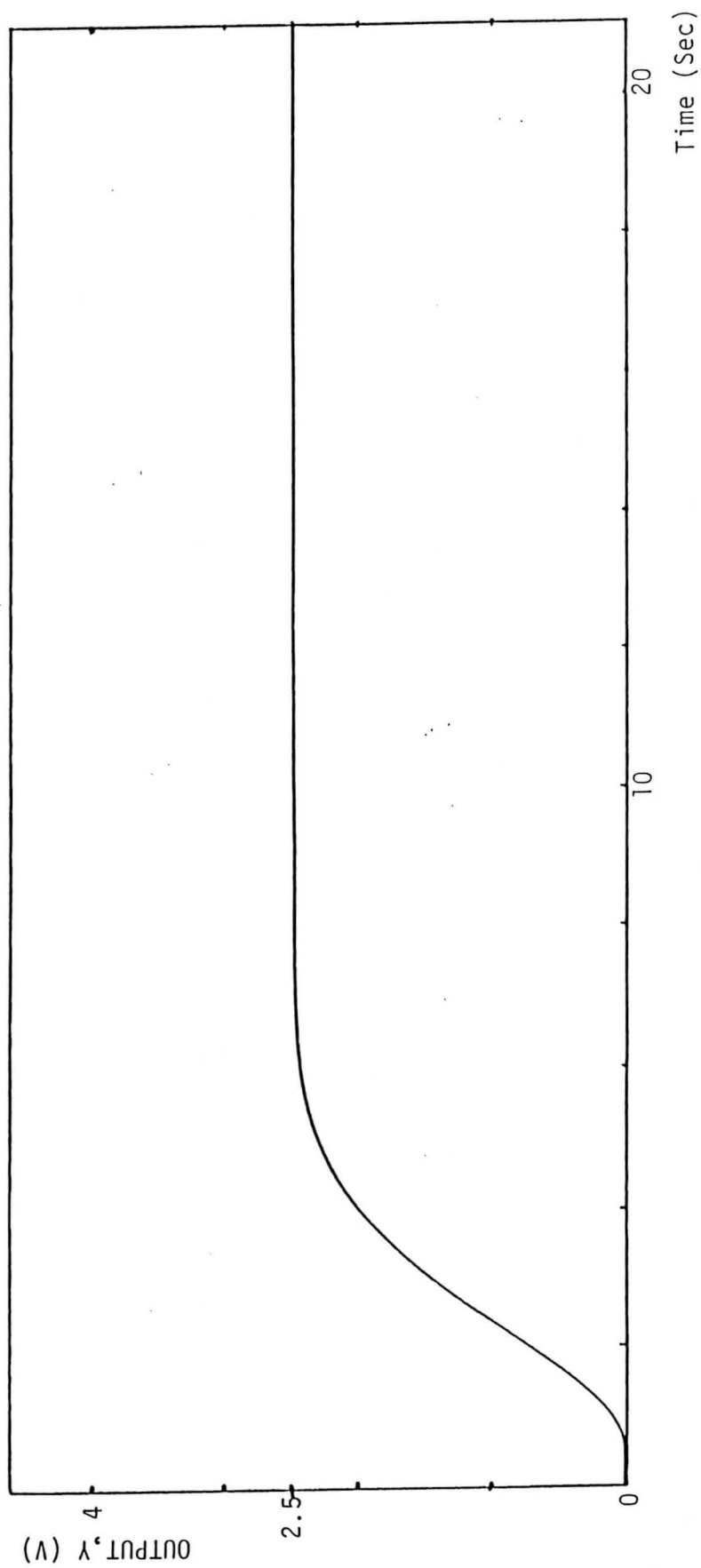


Fig. 4.7 Closed-loop Step Response ($R_k=2.5V$)

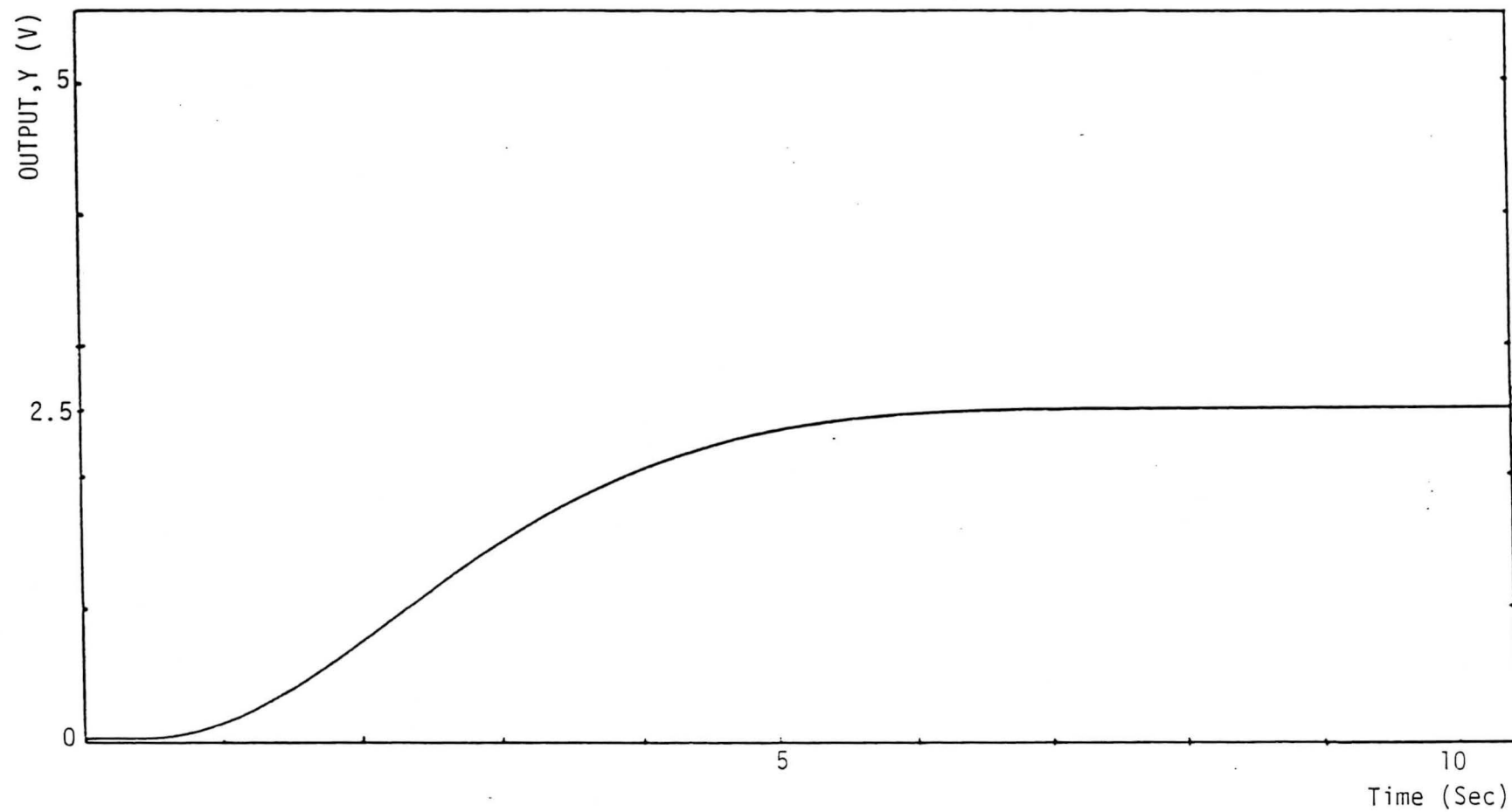


Fig. 4.8 Output Transient Response ($R_k=2.5V$)

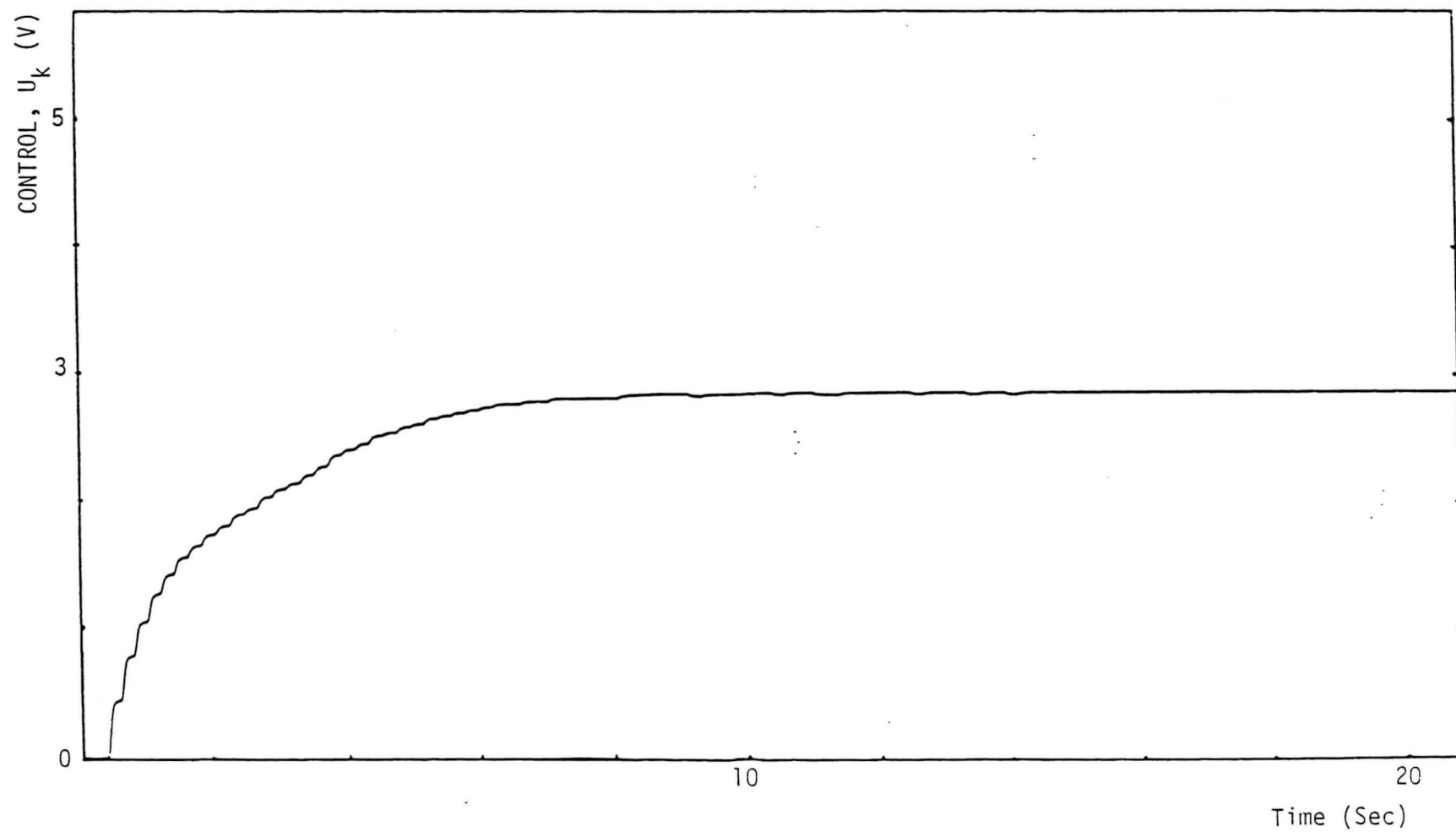


Fig. 4.9 Control Signal ($R_k=2.5V$)

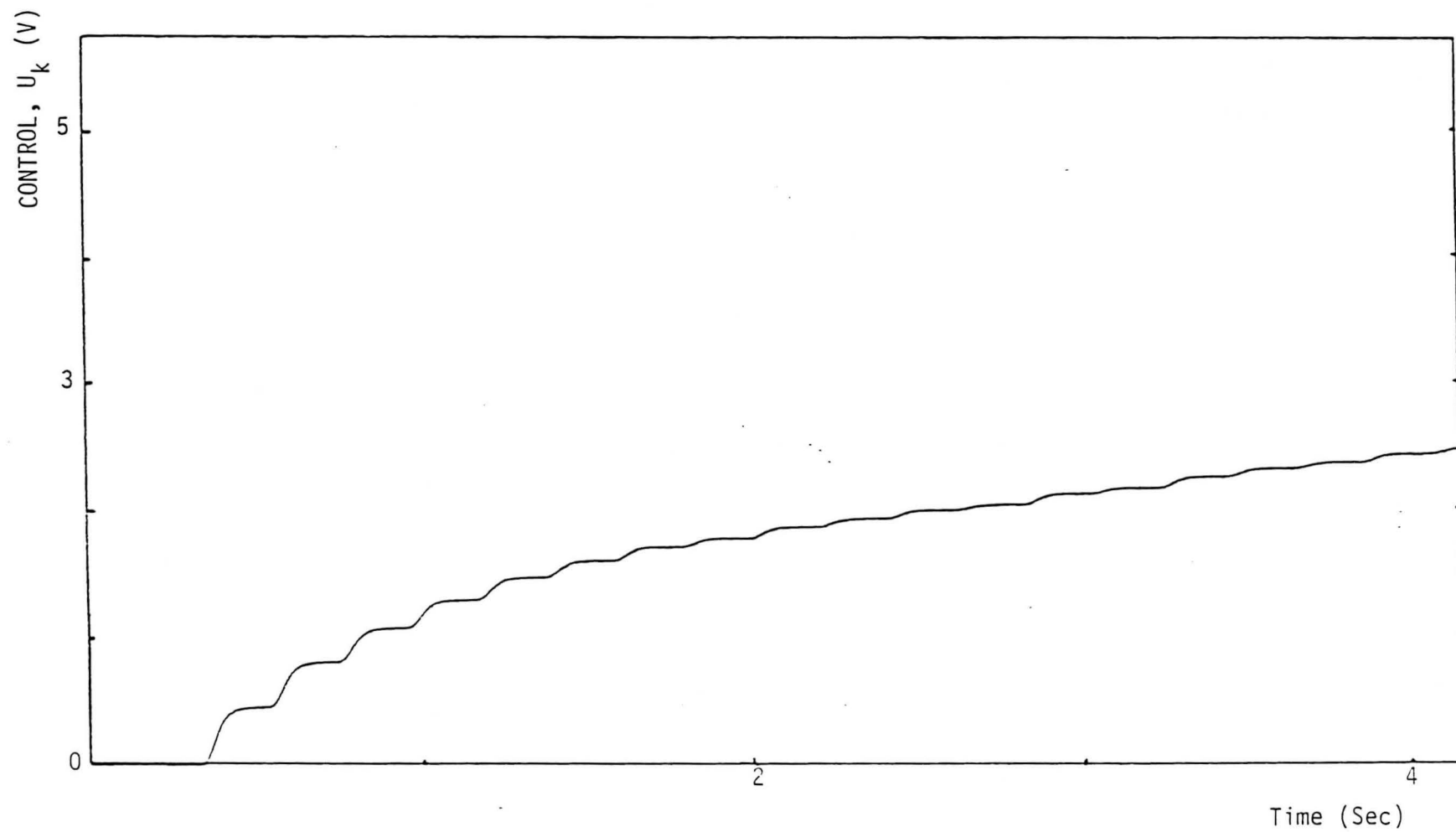


Fig. 4.10 Control Signal Transient Response ($R_k=2.5V$)

All the plots of the output signal are very smooth and both the transient and the steady-state responses are satisfactory. In the responses of the control signal (i.e., Figures 4.5, 4.6, 4.9, and 4.10), one may observe how the dynamics of the pen of the plotter come into play and alter the look of the response between the sampling instances. An attempt to build a filter to increase the bandwidth of the plotter proved to be unsuccessful. It is therefore suggested that a faster plotter be used to plot the responses.

However, the staircase nature of the control signal is far more obvious in the photograph shown in Figure 4.11. This was taken on a Tectronix 2230 Digital Storage Oscilloscope using a Tectronix CRT Camera and a very high-speed film. In this picture, one can see that the transient response of the control signal is as expected: The control starting with zero builds up and reaches its steady-state value without overshooting. Furthermore, the time between two consecutive samples is displayed at the upper-right section of the picture and it equals 0.200 seconds, which is exactly equal to the sampling frequency. This implies that the system is indeed running in real time and that the interface system works properly.

Overall, one can conclude that the digital controller accomplished its purpose as the results obtained from Program CC matched those obtained from the actual implementation of the control algorithm on the general purpose microcomputer used.

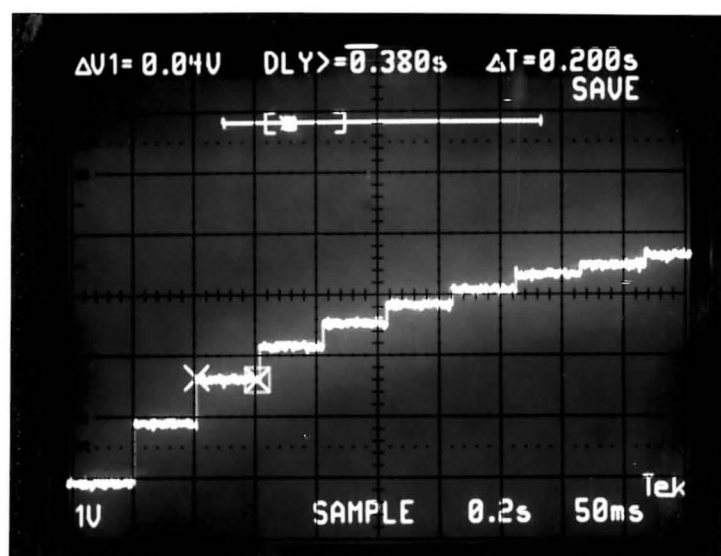


Fig. 4.11 Control Signal Transient Response (CRT)

4.3 Sensitivity Analysis and Tune Up.

In section 4.2, the compensator and observer gain matrices were calculated using the nominal values of the open-loop parameters. If the performance of the digital controller is not satisfactory, the response of the closed-loop system can be easily tuned up. This is done by adjusting the compensator and/or observer gains in the BASIC program (lines 70-100) or even the sampling frequency to accomplish "fine tuning." The results are shown in Figures 4.12 - 4.16. By lowering K_1 , for example, a higher percentage overshoot can be achieved (see Figure 4.12). The response was observed to be most susceptible to observer gain changes (see Figures 4.14 and 4.15).

Thus, a digital controller such as this implemented on the TRS-80 Model IV microcomputer adds some versatility to a digital control system. It is easy to implement and very simple to tune up.

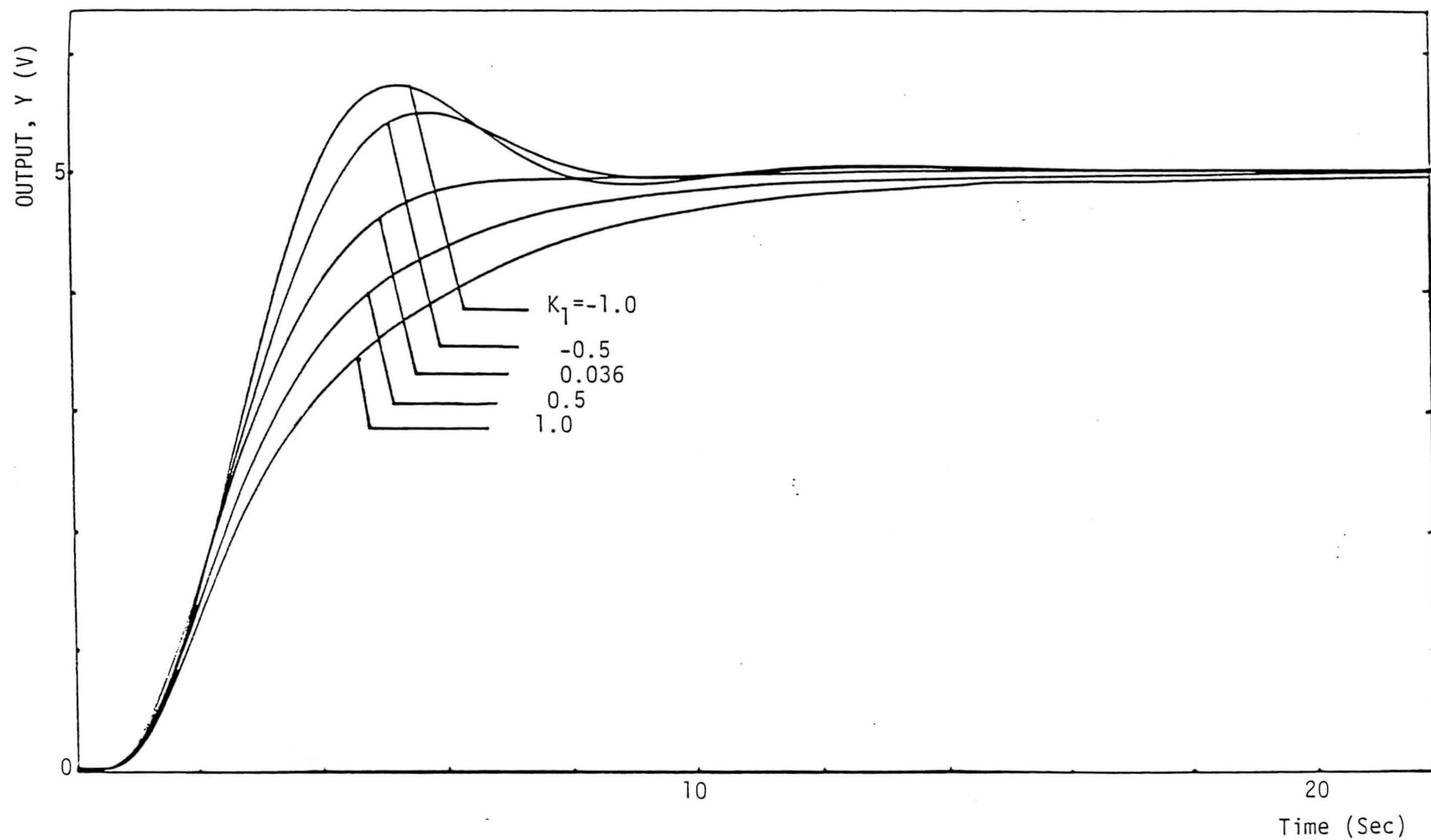


Fig. 4.12 Closed-Loop Response for Various K_1 's

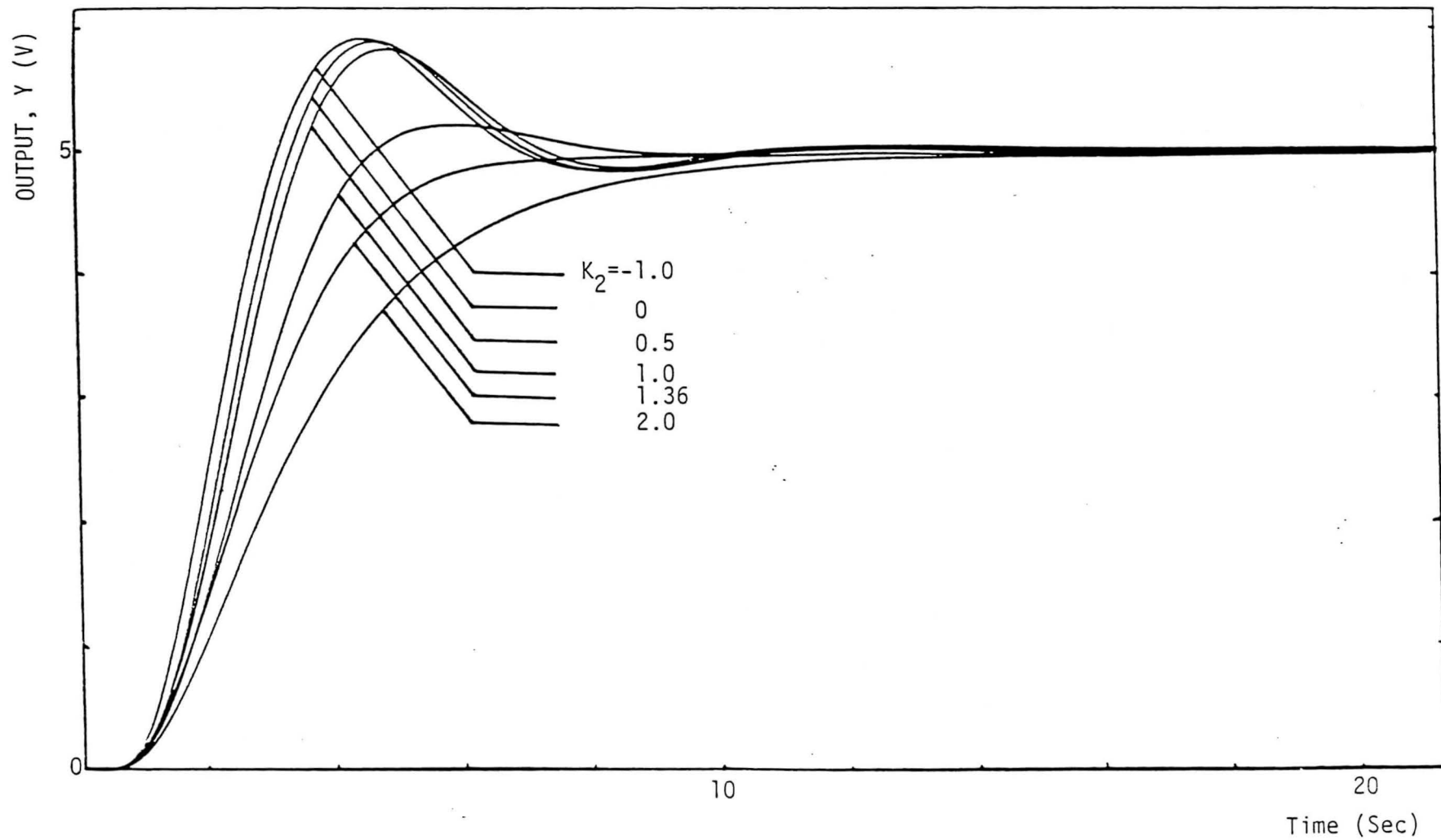


Fig. 4.13 Closed-Loop Response for Various K_2 's

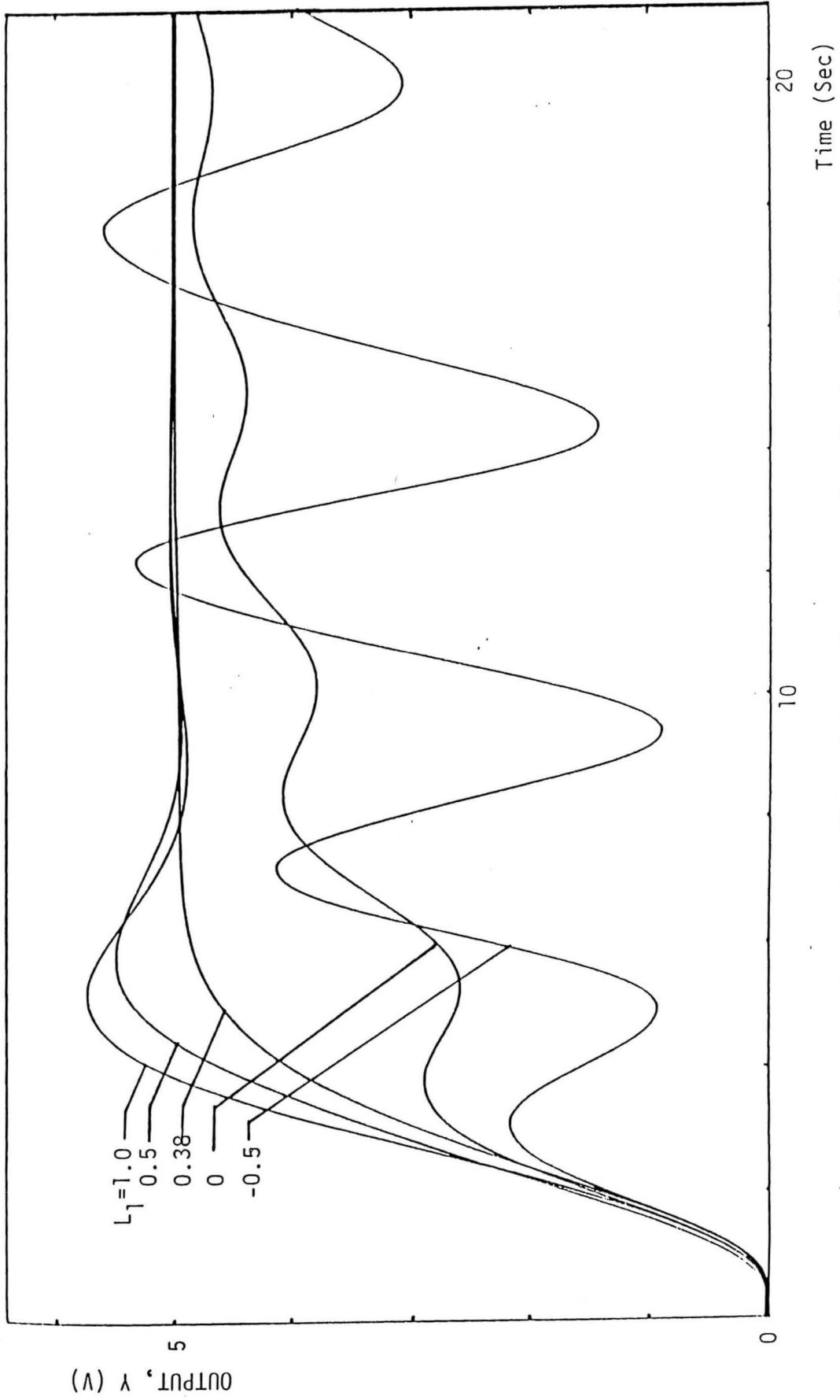


Fig. 4.14 Closed-Loop Response for Various L_1 's

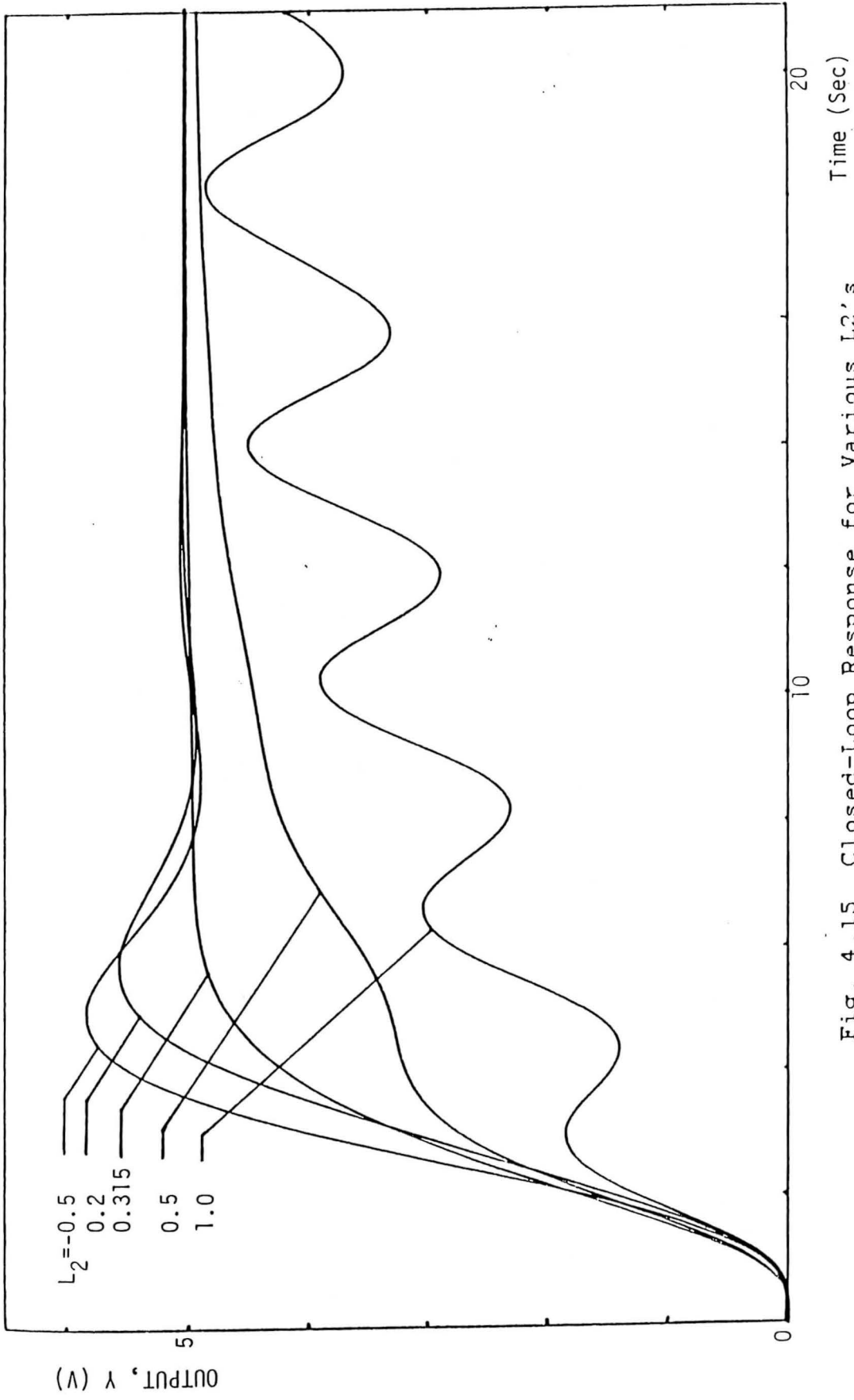


Fig. 4.15 Closed-Loop Response for Various L_2 's

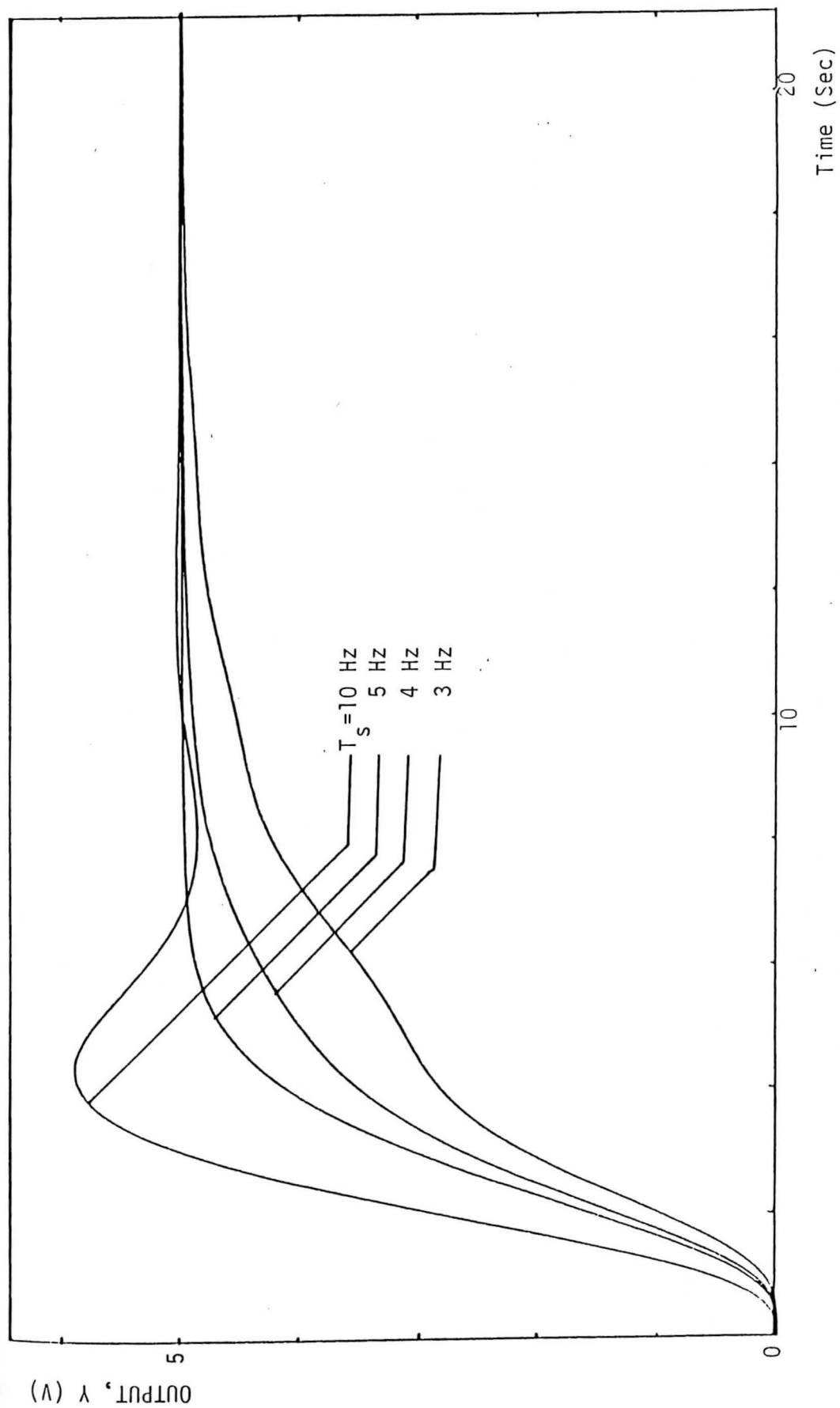


Fig. 4.16 Closed-Loop Response for Various T_s 's

CHAPTER V

CONCLUSION

5.1 SUMMARY

In this thesis, an implementation of a modern control algorithm on a TRS-80 Model IV microcomputer was presented.

Some background in state-variable feedback compensation and the separation principle associated with it was given in Chapter I.

Chapter II dealt with the design of the interface circuitry built to connect a TRS-80 Model IV 8-bit microcomputer to an analog plant.

In Chapter III, the tracking problem was introduced and the technique used to solve it was presented. The method used amounted to building a compensator which included an inner loop and an outer loop. The inner loop used an observer to estimate the state vector to be used in a state-variable feedback control law. On the other hand, the outer loop included an integral controller, which was used in order to achieve a satisfactory tracking performance.

Chapter IV presented an application of the design of Chapter III to a second order system. Program CC was used to carry out the design as well as to simulate the results.

Actual plots of the responses obtained using the Primeline X-Y plotter and a CRT camera indicated that the theoretical and experimental results were amazingly similar. Furthermore, it was pointed out that an unacceptable response can easily be "tuned-up" by adjusting a few parameters by "trial-and-error."

In summary, the experience gained on the TRS-80 Model IV microcomputer can be used with other microcomputers for control applications. Microcomputers are easy to use, very versatile and powerful, and they also are becoming less and less inexpensive.

5.2 Suggestions for Further Work.

To improve the performance of the digital controller presented in this thesis, the following suggestions are made:

A. Suggestions for improving hardware include:

1. A faster computer can be used to achieve higher sampling frequencies. In general, the higher the sampling frequency, the smaller the error between the actual signal and the signal reconstructed using a Zero-Order-Hold device such as an analog-to-digital converter [9].

2. A 16 or 32 bit computer--at the addition of extra cost--can be used to reduce the quantization error. Magnitude quantization on digital control systems may have a significant effect in the steady-

state performance as well as stability of the system [13].

3. A low-cost programmable controller can be used instead of the microcomputer to implement the control algorithm.

B. Suggestions for improving the design are the following:

1. In order to optimize the performance of the controller, the state model can be modified to account for disturbance inputs.

2. An optimum controller can be used to optimize the performance of the system by minimizing a performance index. Also a Kalman filter (i.e., an optimum observer), can be used to estimate the states of the state model, which could also include disturbance inputs, and then use the estimates in the control law [2].

3. A reduced-order observer can be used to reconstruct those states of the system that are not accessible for feedback. The remaining number of the states, being available for direct measurement, should be fed back to the computer using a multiplexer so that they may be used for the control law. However, when a slow computer is used, the state model could be developed in terms of the multiplexed states [14].

4. In order to handle open-loop parameter

changes, an adaptive controller can be designed in order to minimize the servo error in the mean-square sense [15].

APPENDIX A

This appendix contains selected pages from the Data Sheets of the ADC0804 Analog-to-Digital Converter. For more information, reference [7] should be consulted.



ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μ P Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters which use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus, and TRI-STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic needed.

A new differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

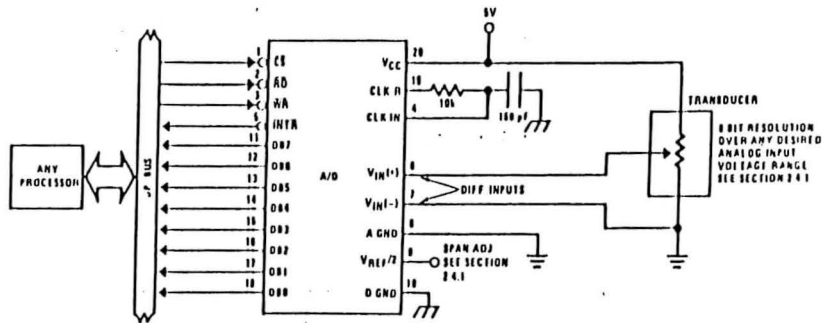
- Compatible with 8080 μ P derivatives—no interfacing logic needed - access time - 135 ns
- Easy Interface to all microprocessors, or operates "stand alone"

- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- Operates ratiometrically or with 5 V_{DD} , 2.5 V_{DD} , or analog span adjusted voltage reference

Key Specifications

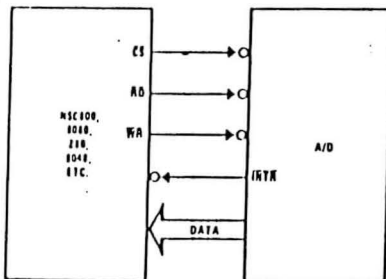
- Resolution 8 bits
- Total error $\pm 1/4$ LSB, $\pm 1/2$ LSB and ± 1 LSB
- Conversion time 100 μ s

Typical Applications



TL/11/5071-1

8080 Interface



TL/11/5071-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)

Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500 V_{DD}$ (No Adjustments)	$V_{REF}/2 =$ No Connection (No Adjustments)
ADC0801	$\pm 1/4$ LSB		
ADC0802		$\pm 1/2$ LSB	
ADC0803	$\pm 1/2$ LSB		
ADC0804		± 1 LSB	
ADC0805			± 1 LSB

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage	
Logic Control Inputs	-0.3V to +18V
At Other Input and Outputs	-0.3V to ($V_{CC} + 0.3V$)
Storage Temperature Range	-65°C to +150°C
Package Dissipation at $T_A = 25^\circ\text{C}$	875 mW
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Conditions (Notes 1 & 2)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
ADC0801/02LJ	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
ADC0801/02/03/04LCJ	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
ADC0801/02/03/05LCN	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
ADC0804LCN	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

Electrical Characteristics

The following specifications apply for $V_{CC} = 5 V_{DC}$, $T_{MIN} \leq T_A \leq T_{MAX}$ and $f_{CLK} = 640 \text{ kHz}$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
ADC0801: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/4$	LSB
ADC0802: Total Unadjusted Error (Note 8)	$V_{REF}/2 = 2.500 V_{DC}$			$\pm 1/2$	LSB
ADC0803: Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			$\pm 1/2$	LSB
ADC0804: Total Unadjusted Error (Note 8)	$V_{REF}/2 = 2.500 V_{DC}$			± 1	LSB
ADC0805: Total Unadjusted Error (Note 8)	$V_{REF}/2$ -No Connection			± 1	LSB
$V_{REF}/2$ Input Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 1.0	8.0 1.3		k Ω k Ω
Analog Input Voltage Range	(Note 4) $V(+)$ or $V(-)$	Gnd-0.05		$V_{CC} + 0.05$	V_{DC}
DC Common-Mode Error	Over Analog Input Voltage Range		$\pm 1/16$	$\pm 1/8$	LSB
Power Supply Sensitivity	$V_{CC} = 5 V_{DC} \pm 10\%$ Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		$\pm 1/16$	$\pm 1/8$	LSB

AC Electrical Characteristics

The following specifications apply for $V_{CC} = 5 V_{DC}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_C	Conversion Time	$f_{CLK} = 640 \text{ kHz}$ (Note 6)	103		114	μs
T_C	Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
f_{CLK}	Clock Frequency	$V_{CC} = 5V$, (Note 5)	100	640	1460	kHz
	Clock Duty Cycle	(Note 5)	40		60	%
CR	Conversion Rate in Free-Running Mode	INTR tied to WR with $\overline{CS} = 0 V_{DC}$, $f_{CLK} = 640 \text{ kHz}$			8770	conv/s
$t_{W(WR)L}$	Width of WR Input (Start Pulse Width)	$\overline{CS} = 0 V_{DC}$ (Note 7)	100			ns
t_{ACC}	Access Time (Delay from Falling Edge of RD to Output Data Valid)	$C_L = 100 \text{ pF}$		135	200	ns
t_{IH}, t_{OH}	TRI-STATE Control (Delay from Rising Edge of RD to Hi-Z State)	$C_L = 10 \text{ pF}$, $R_L = 10k$ (See TRI-STATE Test Circuits)		125	200	ns
t_{WL}, t_{RI}	Delay from Falling Edge of WR or RD to Reset of INTR			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF

APPENDIX B

The following appendix contains selected pages from the Data Sheets of the DAC0806 Digital-to-Analog Converter. For more information, the interested reader should consult reference [7].



DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ± 1 LSB of $255 I_{REF}/256$. Relative accuracies of better than $\pm 0.19\%$ assure 8-bit monotonicity and linearity while zero level output current of less than $4 \mu A$ provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

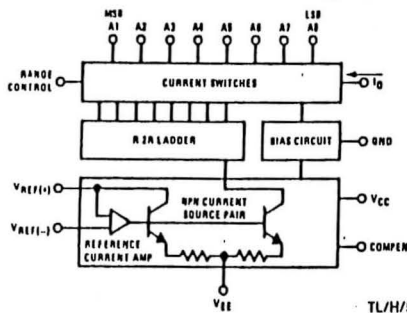
The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the

MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

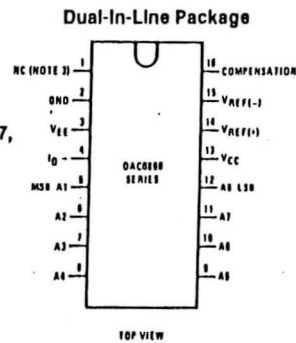
- Relative accuracy: $\pm 0.19\%$ error maximum (DAC0808)
- Full scale current match: ± 1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: $8 \text{ mA}/\mu\text{s}$
- Power supply voltage range: $\pm 4.5V$ to $\pm 18V$
- Low power consumption: 33 mW @ $\pm 5V$

Block and Connection Diagrams



TL/H/5687-1

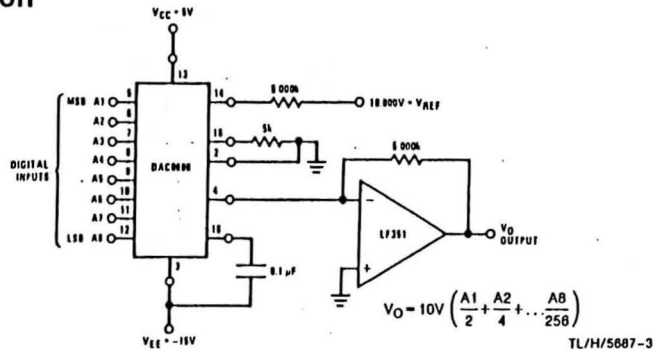
Order Number
DAC0808, DAC0807,
or DAC0806
See NS Package
J16A
or N16A



TOP VIEW

TL/H/5687-2

Typical Application



TL/H/5687-3

FIGURE 1. +10V Output Digital to Analog Converter

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*			
		J PACKAGE (J16A)		N PACKAGE (N16A)	
8-bit	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	DAC0808LJ	MC1508L8	DAC0808LCN	MC1408P8
8-bit	$0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$	DAC0808LCJ	MC1408L8	DAC0807LCN	MC1408P7
7-bit	$0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$	DAC0807LCJ	MC1408L7	DAC0806LCN	MC1408P6
6-bit	$0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$	DAC0806LCJ	MC1408L6		

*Note: Devices may be ordered by using either order number.

Absolute Maximum Ratings

Power Supply Voltage		Power Dissipation (Package Limitation)	1000 mW
V_{CC}	+18 V _{DC}	Derate above $T_A = 25^\circ\text{C}$	6.7 mW/ $^\circ\text{C}$
V_{EE}	-18 V _{DC}	Operating Temperature Range	
Digital Input Voltage, V_{5-V12}	-10 V _{DC} to +18 V _{DC}	DAC0808L	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$
Applied Output Voltage, V_O	-11 V _{DC} to +18 V _{DC}	DAC0808LC Series	$0 \leq T_A \leq +75^\circ\text{C}$
Reference Current, I_{14}	5 mA	Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Reference Amplifier Inputs, V_{14}, V_{15}	V_{CC}, V_{EE}		

Electrical Characteristics

($V_{CC} = 5\text{V}$, $V_{EE} = -15\text{V}_{DC}$, $V_{REF}/R_{14} = 2\text{mA}$, DAC0808: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, DAC0808C, DAC0807C, DAC0806C, $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O) DAC0808L (LM1508-8), DAC0808LC (LM1408-8) DAC0807LC (LM1408-7), (Note 1) DAC0806LC (LM1408-6), (Note 1) Settling Time to Within $\frac{1}{2}$ LSB (Includes I_{PL1})	(Figure 4) $T_A = 25^\circ\text{C}$ (Note 2), (Figure 5)			± 0.19 ± 0.39 ± 0.70	% % % ns
t_{PLH}, t_{FALL}	Propagation Delay Time	$T_A = 25^\circ\text{C}$, (Figure 5)		30	100	ns
TC_{IO}	Output Full Scale Current Drift			± 20		ppm/ $^\circ\text{C}$
MSB V_{IH} V_{IL}	Digital Input Logic Levels High Level, Logic "1" Low Level, Logic "0"	(Figure 3)	2		0.8	V_{DC} V_{DC}
MSB	Digital Input Current High Level Low Level	(Figure 3) $V_{IH} = 5\text{V}$ $V_{IL} = 0.8\text{V}$		0 -0.003	0.040 -0.8	mA mA
I_{15}	Reference Input Bias Current	(Figure 3)		-1	-3	μA
	Output Current Range	(Figure 3) $V_{EE} = -5\text{V}$ $V_{EE} = -15\text{V}$, $T_A = 25^\circ\text{C}$	0 0	2.0 2.0	2.1 4.2	mA mA
I_O	Output Current	$V_{REF} = 2.000\text{V}$, $R_{14} = 1000\Omega$, (Figure 3)	1.9	1.99	2.1	mA
	Output Current, All Bits Low	(Figure 3)		0	4	μA
	Output Voltage Compliance (Note 3) $V_{EE} = -5\text{V}$, $I_{REF} = 1\text{mA}$ V_{EE} Below -10V	$E_r \leq 0.10\%$, $T_A = 25^\circ\text{C}$			-0.55, ± 0.4 -5.0, ± 0.4	V_{DC} V_{DC}
$S_{II_{REF}}$	Reference Current Slew Rate	(Figure 6)	4	8		mA/ μs
	Output Current Power Supply Sensitivity	$-5\text{V} \leq V_{EE} \leq -16.5\text{V}$		0.05	2.7	$\mu\text{A}/\text{V}$
I_{CC} I_{EE}	Power Supply Current (All Bits Low)	(Figure 3)		2.3 -4.3	22 -13	mA mA
V_{CC} V_{EE}	Power Supply Voltage Range	$T_A = 25^\circ\text{C}$, (Figure 3)	4.5 -4.5	5.0 -15	5.5 -16.5	V_{DC} V_{DC}
	Power Dissipation All Bits Low	$V_{CC} = 5\text{V}$, $V_{EE} = -5\text{V}$ $V_{CC} = 5\text{V}$, $V_{EE} = -15\text{V}$ $V_{CC} = 15\text{V}$, $V_{EE} = -5\text{V}$ $V_{CC} = 15\text{V}$, $V_{EE} = -15\text{V}$		33 106 90 160	170 305	mW mW mW mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.

Note 2: All bits switched.

Note 3: Range control is not required.

APPENDIX C

The equations governing the closed-loop system assuming that the actual state vector is feedback are

$$X(k+1) = \Phi X(k) + \Gamma U(k) \quad \{A.1\}$$

$$U(k) = -K X(k) + V(k)$$

$$Y(k) = C X(k) \quad \{A.2\}$$

$$\begin{aligned} \text{Thus, } X(k+1) &= \Phi X(k) + \Gamma (-K X(k) + V(k)) \\ &= (\Phi - \Gamma K) X(k) + \Gamma V(k) \end{aligned} \quad \{A.3\}$$

When a full-state observer is present one gets

$$X(k+1) = \Phi X(k) + \Gamma U(k)$$

$$\hat{X}(k+1) = (\Phi - L C - \Gamma K) \hat{X}(k) + L Y(k) + M V(k) \quad \{A.4\}$$

$$U(k) = -K \hat{X}(k) + N V(k) \quad \{A.5\}$$

$$Y(k) = C X(k)$$

Subtracting {A.4} from {A.1} one gets

$$\begin{aligned} \tilde{X}(k+1) &= X(k+1) - \hat{X}(k+1) = (\Phi X(k) + \Gamma U(k)) \\ &\quad - (\Phi - L C - \Gamma K) \hat{X}(k) - L Y(k) - M V(k) \end{aligned} \quad \{A.6\}$$

Rearranging the terms, {A.6} with {A.2} becomes

$$\tilde{X}(k+1) = (\Phi - L C) \hat{X}(k) + (\Gamma N - M) V(k) \quad \{A.7\}$$

Also, {A.1} can be expressed in terms of the new state:

$$\begin{aligned} X(k+1) &= \Phi X(k) + \Gamma U(k) = \Phi X(k) + \Gamma (-K \hat{X}(k) + N U(k)) \\ &= \Phi X(k) - \Gamma K (X(k) - \tilde{X}(k)) + \Gamma N V(k) \\ &= (\Phi - \Gamma K) X(k) + \Gamma K \tilde{X}(k) + \Gamma N V(k) \end{aligned}$$

Thus, the new state-space model (i.e., with the observer) is the following

$$\begin{bmatrix} X(k+1) \\ \tilde{X}(k+1) \end{bmatrix} = \begin{bmatrix} \Phi - \Gamma K & \Gamma K \\ 0 & \Phi - L C \end{bmatrix} \begin{bmatrix} X(k) \\ \tilde{X}(k) \end{bmatrix} + \begin{bmatrix} \Gamma N \\ \Gamma N - M \end{bmatrix} \begin{bmatrix} V(k) \end{bmatrix}$$

and, $Y(k) = \begin{bmatrix} C & 0 \end{bmatrix} \begin{bmatrix} X(k) & \tilde{X}(k) \end{bmatrix}^T$

The observer error, $\tilde{X}(k)$ must be independent of the input.

To accomplish this, one must set

$$\Gamma N - M = 0 \quad \text{or} \quad M = \Gamma N \quad \{A.8\}$$

The state-space model becomes the following

$$\begin{bmatrix} X(k+1) \\ \tilde{X}(k+1) \end{bmatrix} = \begin{bmatrix} \Phi - \Gamma K & \Gamma K \\ 0 & \Phi - L C \end{bmatrix} \begin{bmatrix} X(k) \\ \tilde{X}(k) \end{bmatrix} + \begin{bmatrix} \Gamma N \\ 0 \end{bmatrix} \begin{bmatrix} V(k) \end{bmatrix}$$

and, $Y(k) = \begin{bmatrix} C & 0 \end{bmatrix} \begin{bmatrix} X(k) & \tilde{X}(k) \end{bmatrix}^T$

Also, the transfer function from V to Y is

$$\begin{aligned} & \begin{bmatrix} C & 0 \end{bmatrix} \left[z I - \begin{bmatrix} \Phi - \Gamma K & \Gamma K \\ 0 & \Phi - L C \end{bmatrix} \right]^{-1} \begin{bmatrix} \Gamma N \\ 0 \end{bmatrix} = \\ & = T(z) = C \left[z I - \Phi + \Gamma K \right]^{-1} \Gamma N \quad \{A.9\} \end{aligned}$$

This must equal the transfer function of the closed-loop system without the observer:

$$\hat{G}(z) = C [z I - \Phi + \Gamma K]^{-1} \Gamma = T(z) \quad \{A.10\}$$

From {A.9} and {A.10} one can deduce that

$$\Gamma = \Gamma N \quad \text{or} \quad N = 1. \quad \{A.11\}$$

Combining {A.8} and {A.11}, one gets $M = N \Gamma = \Gamma$.

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